

# Compal confidential

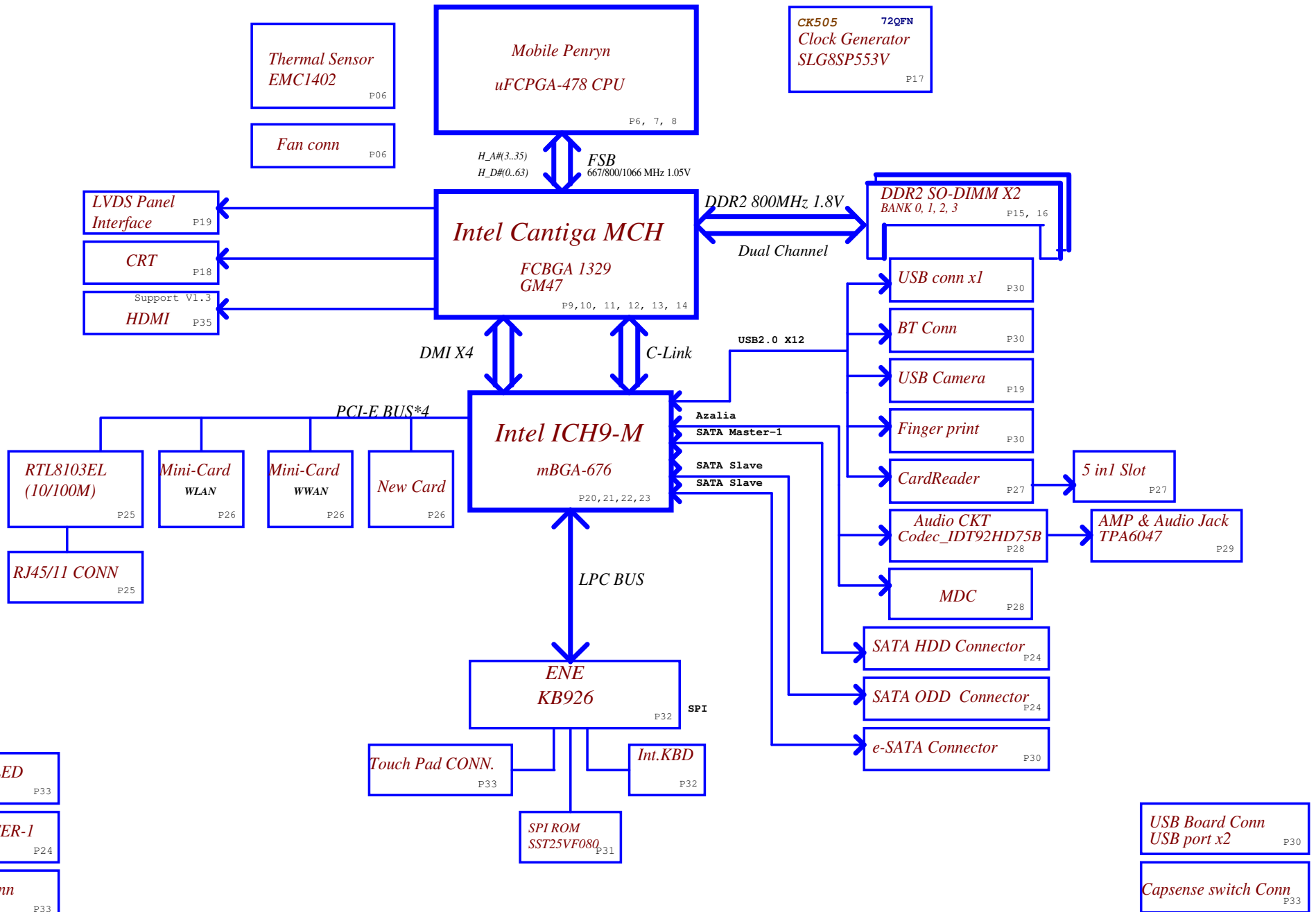
## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_GM+ICH9-M core logic

2009-02-16  
REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	Cover Sheet
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Montevina Consumer UMA



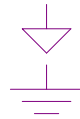
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	Block Diagram
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## Voltage Rails

O MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +2.5VS +1.8V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

## Symbol Note:



: means Digital Ground



: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot
PA @ :	means just reserve for PA
PR @ :	means just reserve for PR

## USB assignment:

USB-0	Right side(with eSATA)
USB-1	Left side
USB-2	Left side
USB-3	Cardreader
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

## PCIe assignment:

PCIe-1	WWAN
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	X
PCIe-6	New Card

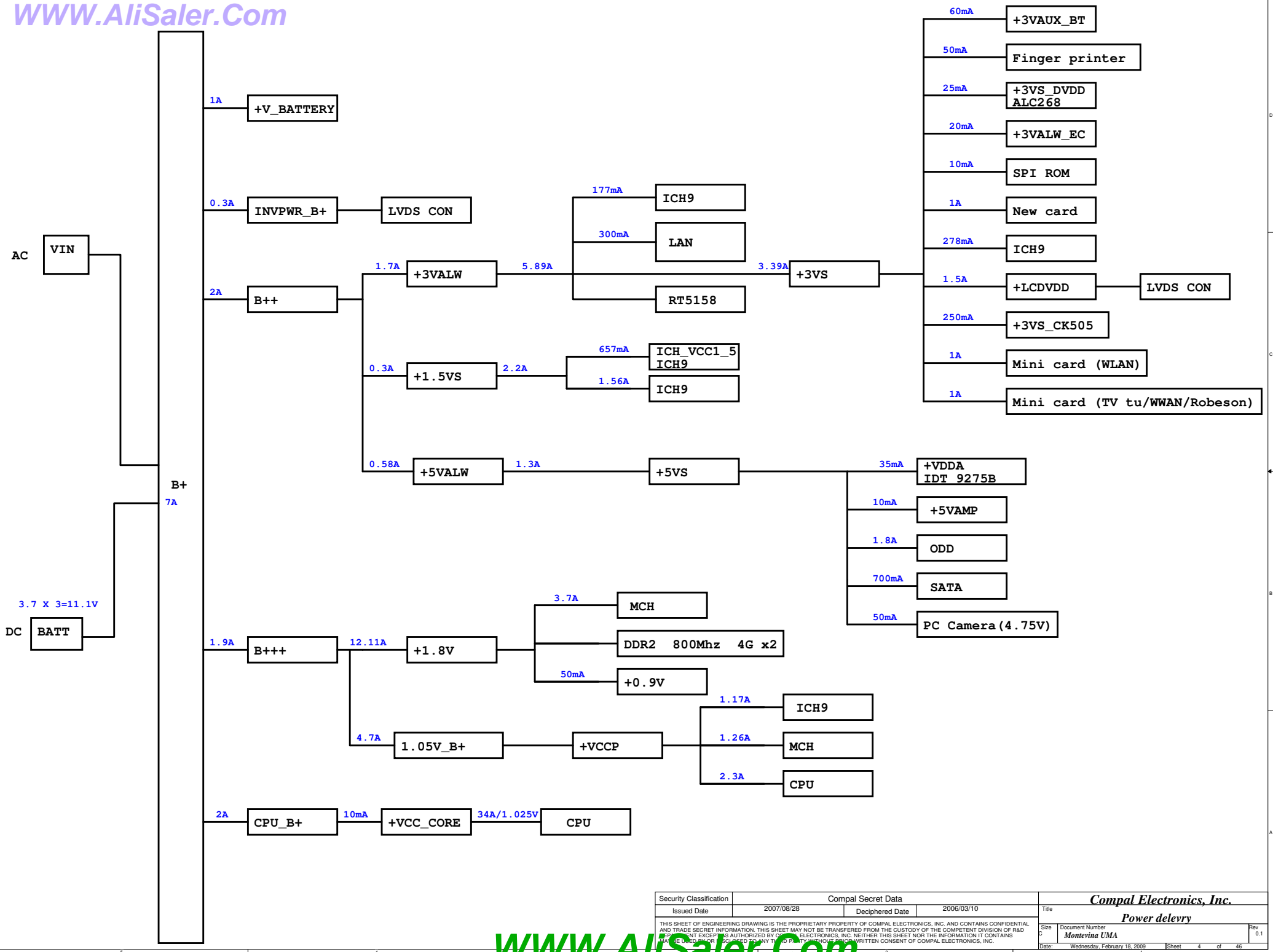
## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10 100 000
DDR SO-DIMM 1	A4	10 100 100
CLOCK GENERATOR (EXT.)	D2	11 010 010

## SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

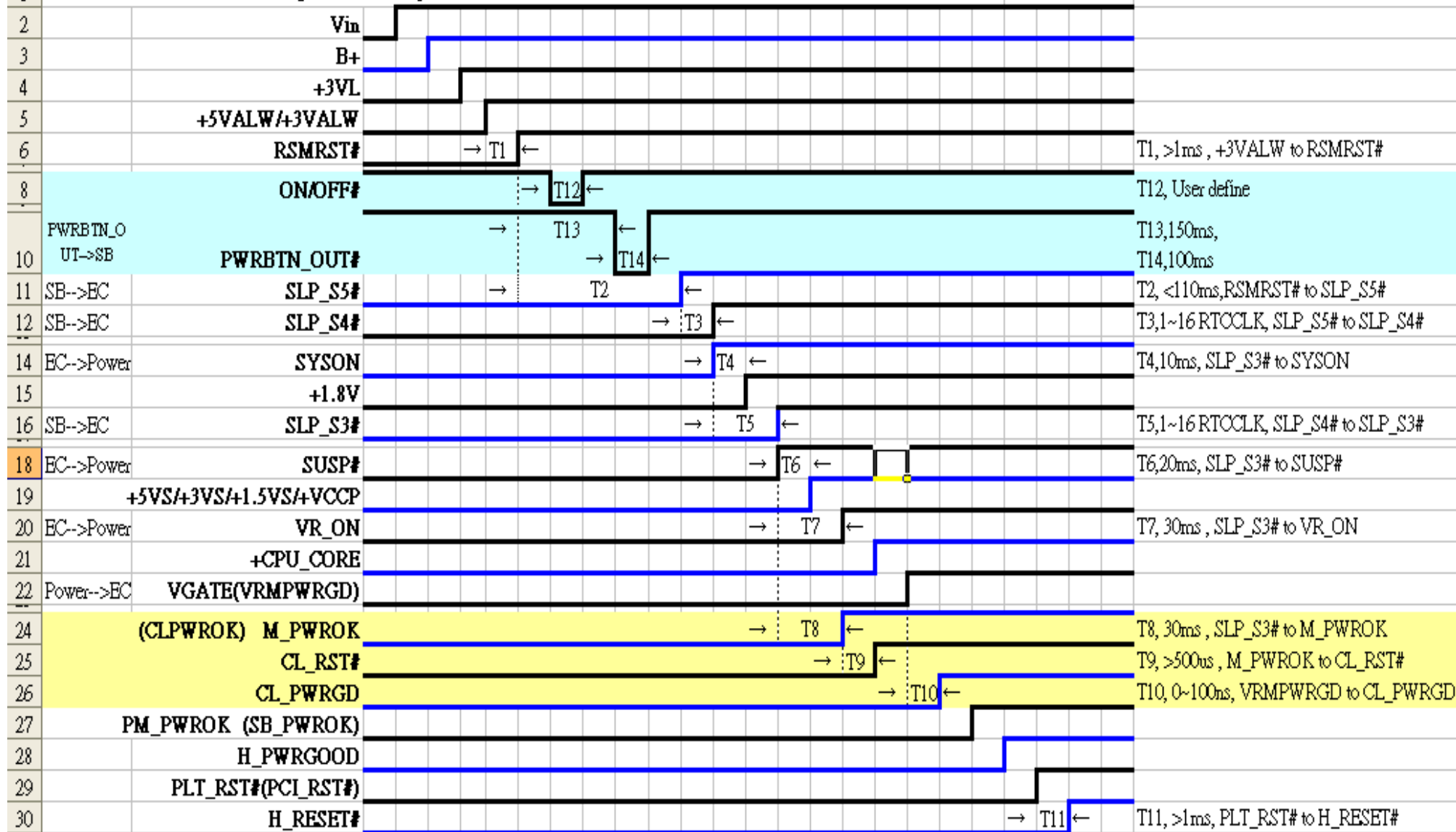
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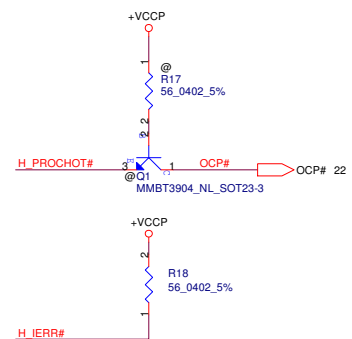
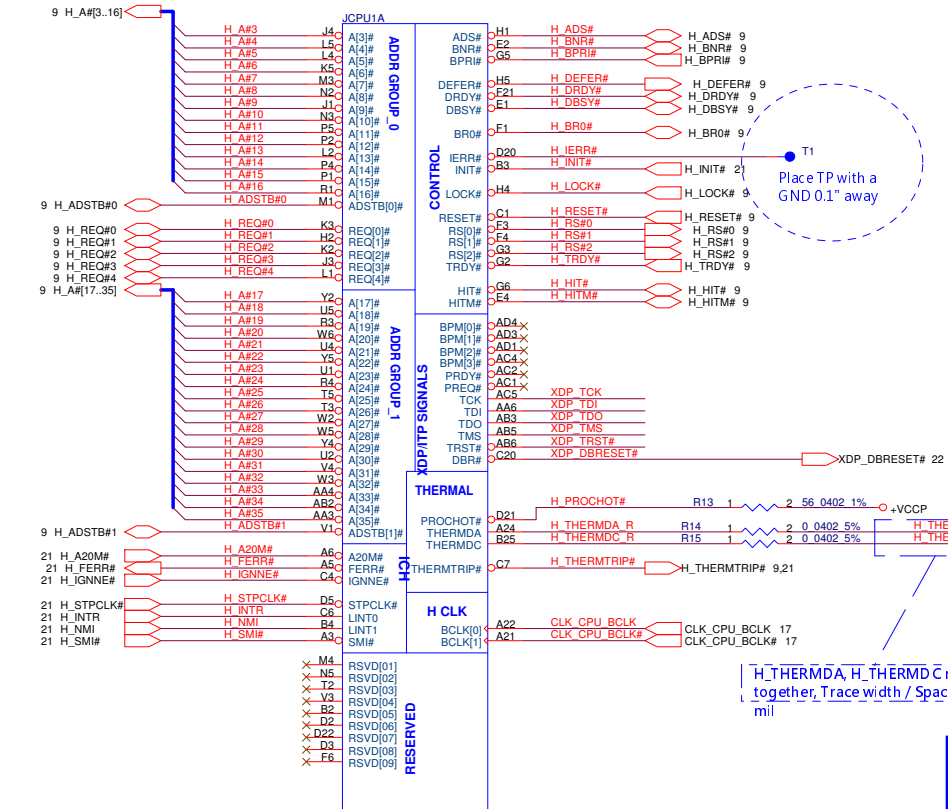


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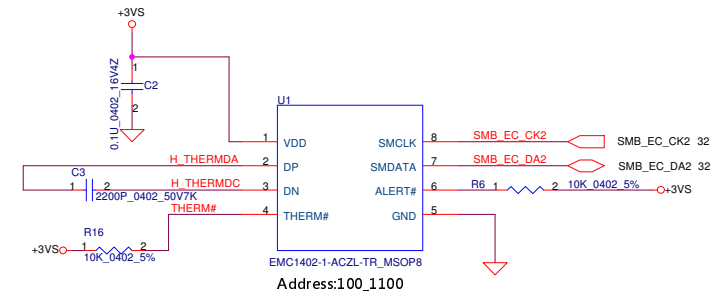
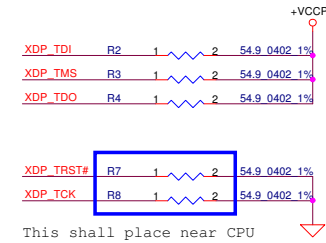
## JAL50 power sequence AC mode

96.09.03.

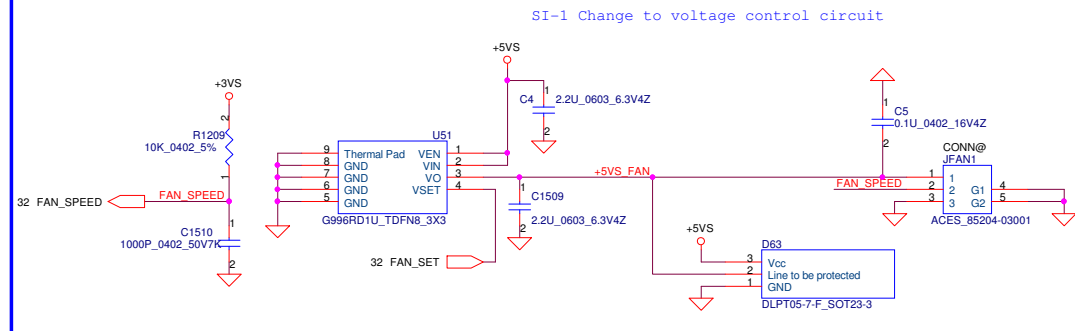




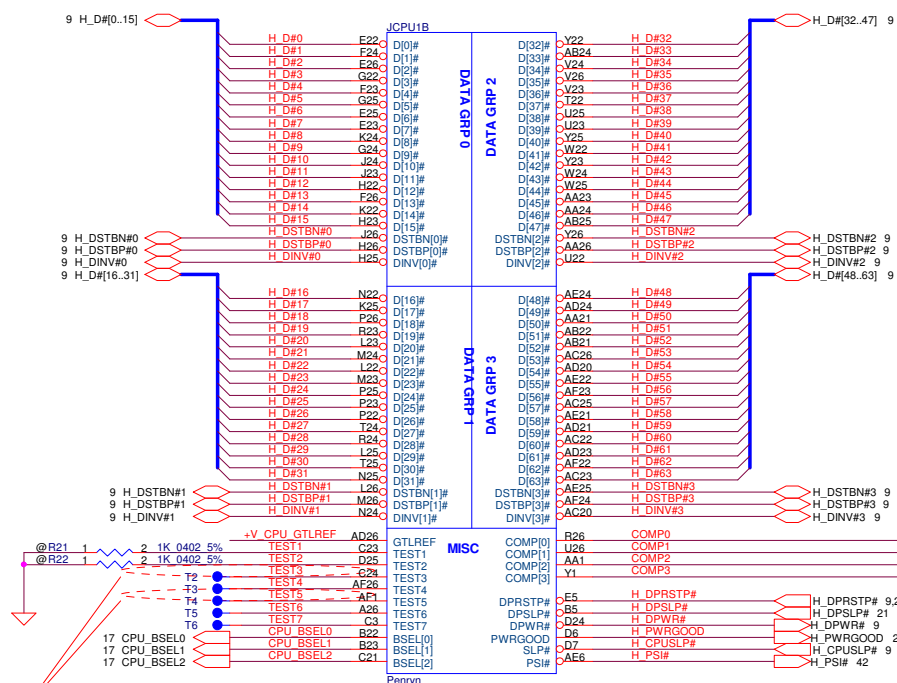
## ITP-XDP Connector



## Fan Control circuit



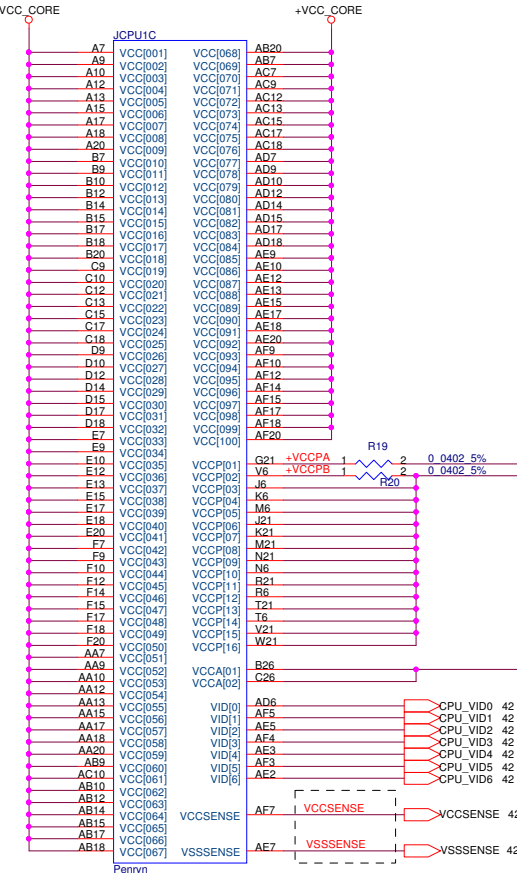
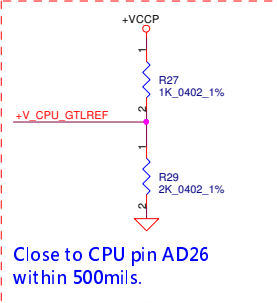
Security Classification				Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date	2006/03/10			Penryn(1/3)-AGTL+/ITP-XDP	
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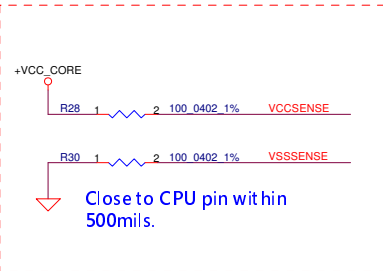
\* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

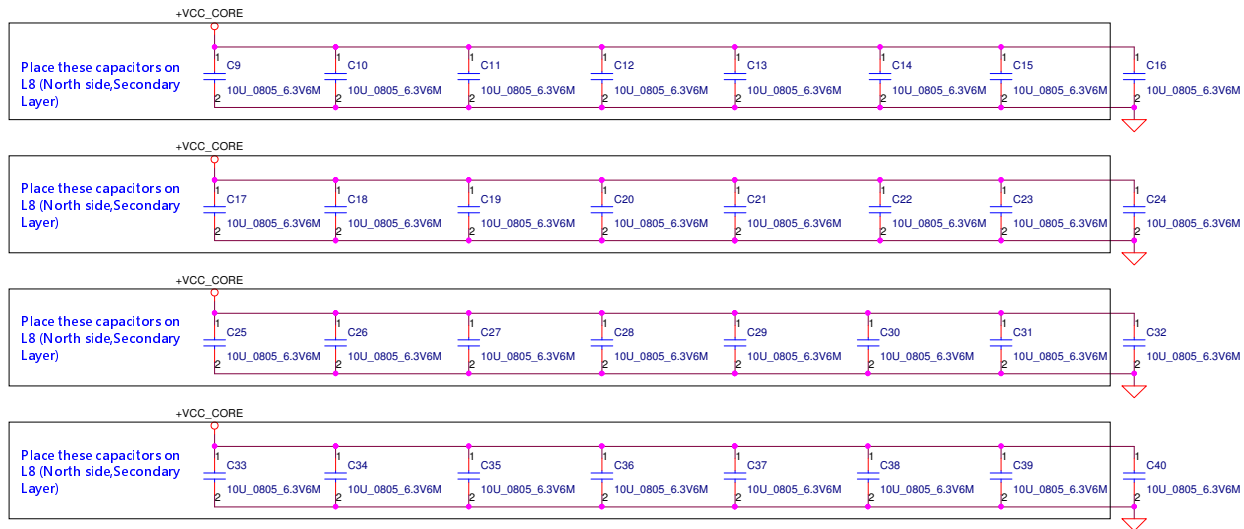
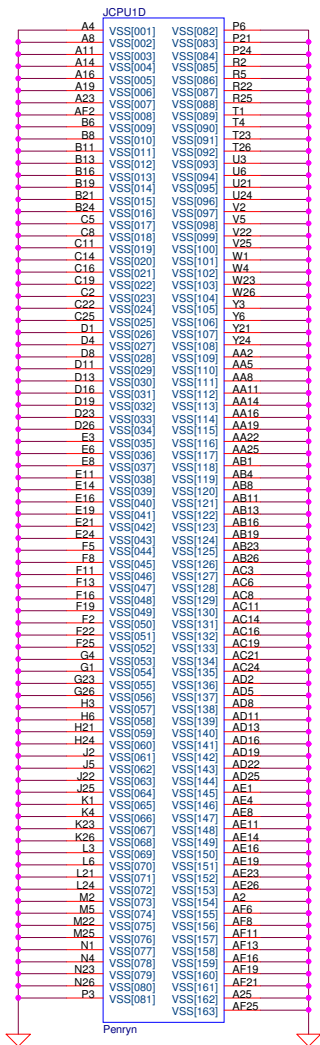
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.

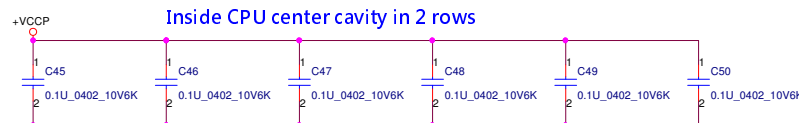
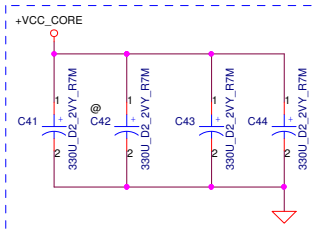




Mid Frequency Decoupling

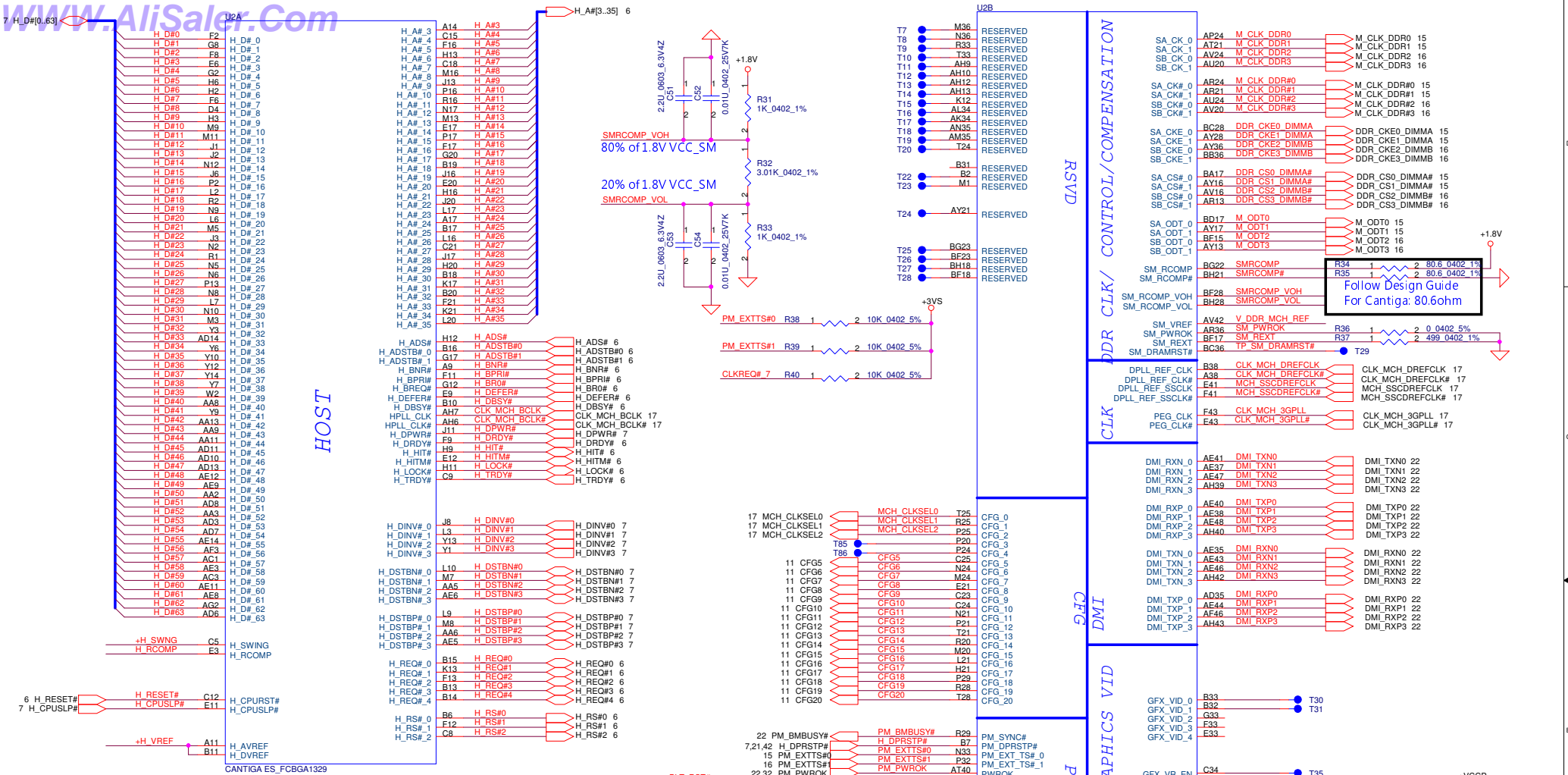
Near CPU CORE regulator

ESR <= 1.5m ohm  
Capacitor > 1980uF



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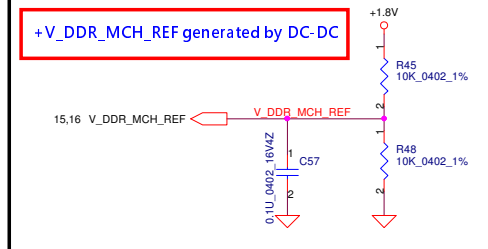
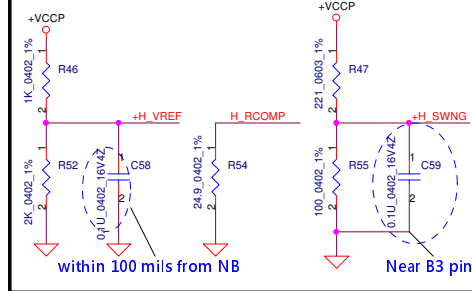


**Layout note:**  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:  
H\_RCOMP / H\_VREF / H\_SWNG  
trace width and spacing is 10/20

Layout Note: V\_DDR\_MCH\_REF trace width and spacing is 20/20.

+V\_DDR\_MCH\_REF generated by DC-DC



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15 DDR\_A\_D[0..63]

U2D

DDR\_A\_D0 AJ38 SA\_DQ\_0  
DDR\_A\_D1 AJ41 SA\_DQ\_1  
DDR\_A\_D2 AN38 SA\_DQ\_2  
DDR\_A\_D3 AJ36 SA\_DQ\_3  
DDR\_A\_D4 AJ36 SA\_DQ\_3  
DDR\_A\_D5 AJ40 SA\_DQ\_4  
DDR\_A\_D6 AM44 SA\_DQ\_6  
DDR\_A\_D7 AM42 SA\_DQ\_7  
DDR\_A\_D8 AM43 SA\_DQ\_8  
DDR\_A\_D9 AN44 SA\_DQ\_8  
DDR\_A\_D10 AU40 SA\_DQ\_10  
DDR\_A\_D11 AN41 SA\_DQ\_11  
DDR\_A\_D12 AT38 SA\_DQ\_11  
DDR\_A\_D13 AN39 SA\_DQ\_12  
DDR\_A\_D14 AU44 SA\_DQ\_14  
DDR\_A\_D15 AU42 SA\_DQ\_15  
DDR\_A\_D16 AV39 SA\_DQ\_17  
DDR\_A\_D17 AY44 SA\_DQ\_16  
DDR\_A\_D18 BA40 SA\_DQ\_18  
DDR\_A\_D19 BA43 SA\_DQ\_18  
DDR\_A\_D20 BD43 SA\_DQ\_19  
DDR\_A\_D21 AV43 SA\_DQ\_21  
DDR\_A\_D22 BB41 SA\_DQ\_22  
DDR\_A\_D23 BC40 SA\_DQ\_23  
DDR\_A\_D24 AV37 SA\_DQ\_24  
DDR\_A\_D25 BD38 SA\_DQ\_25  
DDR\_A\_D26 AV37 SA\_DQ\_26  
DDR\_A\_D27 AT36 SA\_DQ\_27  
DDR\_A\_D28 AV38 SA\_DQ\_28  
DDR\_A\_D29 BB38 SA\_DQ\_29  
DDR\_A\_D30 AV36 SA\_DQ\_30  
DDR\_A\_D31 AW36 SA\_DQ\_31  
DDR\_A\_D32 BD13 SA\_DQ\_32  
DDR\_A\_D33 AU11 SA\_DQ\_34  
DDR\_A\_D34 BC11 SA\_DQ\_35  
DDR\_A\_D35 BA12 SA\_DQ\_36  
DDR\_A\_D36 AU13 SA\_DQ\_37  
DDR\_A\_D37 AV13 SA\_DQ\_38  
DDR\_A\_D38 BD12 SA\_DQ\_39  
DDR\_A\_D39 BC12 SA\_DQ\_40  
DDR\_A\_D40 BB9 SA\_DQ\_41  
DDR\_A\_D41 BA9 SA\_DQ\_42  
DDR\_A\_D42 AU10 SA\_DQ\_43  
DDR\_A\_D43 AV9 SA\_DQ\_44  
DDR\_A\_D44 BA11 SA\_DQ\_45  
DDR\_A\_D45 BD9 SA\_DQ\_46  
DDR\_A\_D46 AV8 SA\_DQ\_47  
DDR\_A\_D47 BA6 SA\_DQ\_48  
DDR\_A\_D48 AV5 SA\_DQ\_49  
DDR\_A\_D49 AT9 SA\_DQ\_50  
DDR\_A\_D50 AT9 SA\_DQ\_51  
DDR\_A\_D51 AN8 SA\_DQ\_52  
DDR\_A\_D52 AU5 SA\_DQ\_53  
DDR\_A\_D53 AU6 SA\_DQ\_54  
DDR\_A\_D54 AT5 SA\_DQ\_55  
DDR\_A\_D55 AN10 SA\_DQ\_56  
DDR\_A\_D56 AM11 SA\_DQ\_57  
DDR\_A\_D57 AM5 SA\_DQ\_58  
DDR\_A\_D58 AJ9 SA\_DQ\_59  
DDR\_A\_D59 AJ8 SA\_DQ\_60  
DDR\_A\_D60 AN12 SA\_DQ\_61  
DDR\_A\_D61 AM13 SA\_DQ\_62  
DDR\_A\_D62 AJ11 SA\_DQ\_63  
DDR\_A\_D63 AJ12 SA\_DQ\_63

DDR SYSTEM MEMORY A

SA\_BS\_0  
SA\_BS\_1  
SA\_BS\_2  
SA\_RAS#  
SA\_CAS#  
SA\_WE#

SA\_DM\_0  
SA\_DM\_1  
SA\_DM\_2  
SA\_DM\_3  
SA\_DM\_4  
SA\_DM\_5  
SA\_DM\_6  
SA\_DM\_7

SA\_DQS\_0  
SA\_DQS\_1  
SA\_DQS\_2  
SA\_DQS\_3  
SA\_DQS\_4  
SA\_DQS\_5  
SA\_DQS\_6  
SA\_DQS\_7

SA\_DQS#\_0  
SA\_DQS#\_1  
SA\_DQS#\_2  
SA\_DQS#\_3  
SA\_DQS#\_4  
SA\_DQS#\_5  
SA\_DQS#\_6  
SA\_DQS#\_7

SA\_MA\_0  
SA\_MA\_1  
SA\_MA\_2  
SA\_MA\_3  
SA\_MA\_4  
SA\_MA\_5  
SA\_MA\_6  
SA\_MA\_7  
SA\_MA\_8  
SA\_MA\_9  
SA\_MA\_10  
SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14

SA\_MA\_0  
SA\_MA\_1  
SA\_MA\_2  
SA\_MA\_3  
SA\_MA\_4  
SA\_MA\_5  
SA\_MA\_6  
SA\_MA\_7  
SA\_MA\_8  
SA\_MA\_9  
SA\_MA\_10  
SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14

SA\_MA\_0  
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SA\_MA\_3  
SA\_MA\_4  
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SA\_MA\_6  
SA\_MA\_7  
SA\_MA\_8  
SA\_MA\_9  
SA\_MA\_10  
SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14

SA\_MA\_0  
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SA\_MA\_2  
SA\_MA\_3  
SA\_MA\_4  
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SA\_MA\_7  
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SA\_MA\_11  
SA\_MA\_12  
SA\_MA\_13  
SA\_MA\_14

CANTIGA ES\_FCBGA1329

16 DDR\_B\_D[0..63]

U2E

DDR\_B\_D0 AK47 SB\_DQ\_0  
DDR\_B\_D1 AH46 SB\_DQ\_1  
DDR\_B\_D2 AP47 SB\_DQ\_2  
DDR\_B\_D3 AF40 SB\_DQ\_3  
DDR\_B\_D4 AJ46 SB\_DQ\_4  
DDR\_B\_D5 AJ48 SB\_DQ\_5  
DDR\_B\_D6 AM48 SB\_DQ\_6  
DDR\_B\_D7 AF48 SB\_DQ\_7  
DDR\_B\_D8 AU47 SB\_DQ\_8  
DDR\_B\_D9 AU46 SB\_DQ\_9  
DDR\_B\_D10 BA48 SB\_DQ\_10  
DDR\_B\_D11 BA48 SB\_DQ\_11  
DDR\_B\_D12 AT47 SB\_DQ\_12  
DDR\_B\_D13 AR47 SB\_DQ\_13  
DDR\_B\_D14 BA47 SB\_DQ\_14  
DDR\_B\_D15 BC47 SB\_DQ\_15  
DDR\_B\_D16 BC46 SB\_DQ\_16  
DDR\_B\_D17 BC44 SB\_DQ\_17  
DDR\_B\_D18 BG43 SB\_DQ\_18  
DDR\_B\_D19 BF43 SB\_DQ\_19  
DDR\_B\_D20 BF45 SB\_DQ\_20  
DDR\_B\_D21 BC41 SB\_DQ\_21  
DDR\_B\_D22 BF40 SB\_DQ\_22  
DDR\_B\_D23 BF41 SB\_DQ\_23  
DDR\_B\_D24 BC38 SB\_DQ\_24  
DDR\_B\_D25 BF38 SB\_DQ\_25  
DDR\_B\_D26 BH35 SB\_DQ\_26  
DDR\_B\_D27 BG35 SB\_DQ\_27  
DDR\_B\_D28 BH40 SB\_DQ\_28  
DDR\_B\_D29 BC39 SB\_DQ\_29  
DDR\_B\_D30 BG34 SB\_DQ\_30  
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DDR\_B\_D36 BH12 SB\_DQ\_36  
DDR\_B\_D37 BF11 SB\_DQ\_37  
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DDR\_B\_D47 BD3 SB\_DQ\_47  
DDR\_B\_D48 AV2 SB\_DQ\_48  
DDR\_B\_D49 AR3 SB\_DQ\_49  
DDR\_B\_D50 AR3 SB\_DQ\_50  
DDR\_B\_D51 AN2 SB\_DQ\_51  
DDR\_B\_D52 AY2 SB\_DQ\_52  
DDR\_B\_D53 AV1 SB\_DQ\_53  
DDR\_B\_D54 AP3 SB\_DQ\_54  
DDR\_B\_D55 AR1 SB\_DQ\_55  
DDR\_B\_D56 AL1 SB\_DQ\_56  
DDR\_B\_D57 AL2 SB\_DQ\_57  
DDR\_B\_D58 AH1 SB\_DQ\_58  
DDR\_B\_D59 AM2 SB\_DQ\_59  
DDR\_B\_D60 AM3 SB\_DQ\_60  
DDR\_B\_D61 AH3 SB\_DQ\_61  
DDR\_B\_D62 AH3 SB\_DQ\_62  
DDR\_B\_D63 AJ3 SB\_DQ\_63

DDR SYSTEM MEMORY B

CANTIGA ES\_FCBGA1329

SB\_BS\_0  
SB\_BS\_1  
SB\_BS\_2  
SB\_RAS#  
SB\_CAS#  
SB\_WE#

SB\_DM\_0  
SB\_DM\_1  
SB\_DM\_2  
SB\_DM\_3  
SB\_DM\_4  
SB\_DM\_5  
SB\_DM\_6  
SB\_DM\_7

SB\_DQS\_0  
SB\_DQS\_1  
SB\_DQS\_2  
SB\_DQS\_3  
SB\_DQS\_4  
SB\_DQS\_5  
SB\_DQS\_6  
SB\_DQS\_7

SB\_DQS#\_0  
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SB\_DQS#\_7

SB\_MA\_0  
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SB\_MA\_11  
SB\_MA\_12  
SB\_MA\_13  
SB\_MA\_14

BC16 DDR\_B\_BS0  
BB17 DDR\_B\_BS1  
BB33 DDR\_B\_BS2  
AU17 DDR\_B\_RAS#  
BG16 DDR\_B\_CAS#  
BF14 DDR\_B\_WE#

AM47 DDR\_B\_DM0  
AY47 DDR\_B\_DM1  
BD40 DDR\_B\_DM2  
BF35 DDR\_B\_DM3  
BG11 DDR\_B\_DM4  
BA3 DDR\_B\_DM5  
AP1 DDR\_B\_DM6  
AK2 DDR\_B\_DM7

AL47 DDR\_B\_DQS0  
AV48 DDR\_B\_DQS1  
BG41 DDR\_B\_DQS2  
BG37 DDR\_B\_DQS3  
BH9 DDR\_B\_DQS4  
BB2 DDR\_B\_DQS5  
AU1 DDR\_B\_DQS6  
AN6 DDR\_B\_DQS7

AL46 DDR\_B\_DQS#0  
AV47 DDR\_B\_DQS#1  
BH41 DDR\_B\_DQS#2  
BH37 DDR\_B\_DQS#3  
BG9 DDR\_B\_DQS#4  
BC2 DDR\_B\_DQS#5  
AT2 DDR\_B\_DQS#6  
AN5 DDR\_B\_DQS#7

AV17 DDR\_B\_MA0  
BA25 DDR\_B\_MA1  
BC25 DDR\_B\_MA2  
AU25 DDR\_B\_MA3  
AW25 DDR\_B\_MA4  
BB28 DDR\_B\_MA5  
AU28 DDR\_B\_MA6  
AW28 DDR\_B\_MA7

AT33 DDR\_B\_MA8  
BD33 DDR\_B\_MA9  
BB16 DDR\_B\_MA10  
AW33 DDR\_B\_MA11  
AY33 DDR\_B\_MA12  
BH15 DDR\_B\_MA13  
AU33 DDR\_B\_MA14

AT33 DDR\_B\_MA8  
BD33 DDR\_B\_MA9  
BB16 DDR\_B\_MA10  
AW33 DDR\_B\_MA11  
AY33 DDR\_B\_MA12  
BH15 DDR\_B\_MA13  
AU33 DDR\_B\_MA14

AT33 DDR\_B\_MA8  
BD33 DDR\_B\_MA9  
BB16 DDR\_B\_MA10  
AW33 DDR\_B\_MA11  
AY33 DDR\_B\_MA12  
BH15 DDR\_B\_MA13  
AU33 DDR\_B\_MA14

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Follow Intel DG & Checklist

Follow Intel DG & Checklist

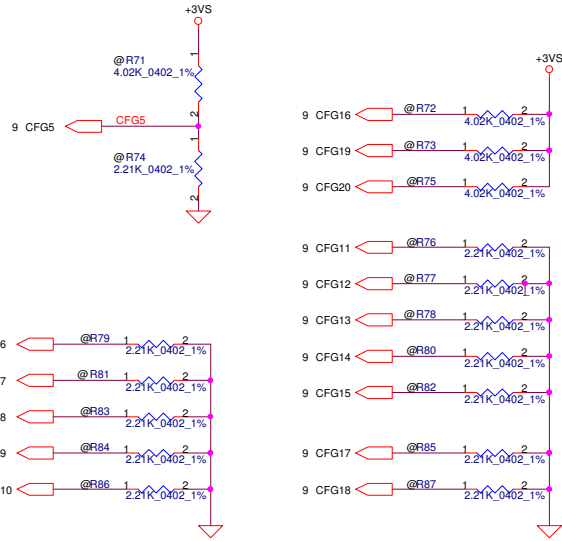
Follow Intel DG & Checklist

For 3G  
WWAN

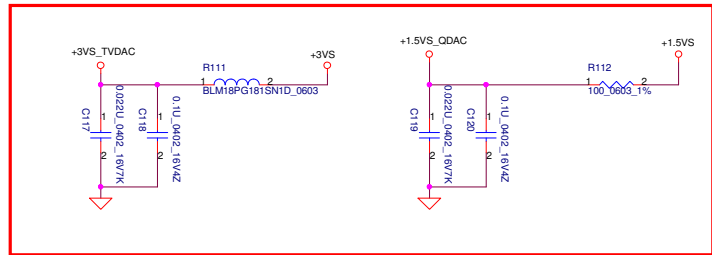
For 3G  
WWAN

## Strap Pin Table

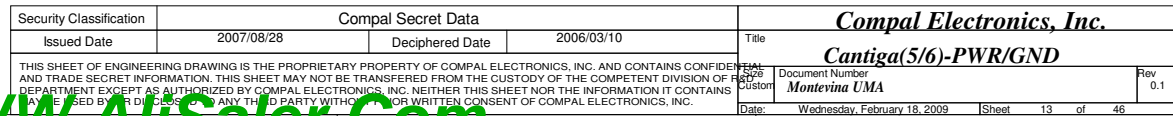
CFG[2:0] FSB Freq select	000 = FSB 800MHz 001 = FSB 800MHz 010 = FSB 800MHz 011 = FSB 800MHz 100 = FSB 800MHz 101 = FSB 800MHz 110 = FSB 800MHz 111 = FSB 800MHz
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 3
CFG6	0 = The iTPM Host Interface is enabled 1 = The iTPM Host Interface is disabled
CFG7 (Intel Management Engine Crypto strap)	0 = iTPM chip suite with no confidentiality 1 = iTPM chip suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15 -> 0, 14 -> 1, etc. 1 = Normal Operation, Lane Number in order
CFG10 (PCIe Lookback enable)	0 = Disabled 1 = Enabled
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode 10 = All Z Mode 11 = Normal (Default)
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation, number in order 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operating 1 = PCIe/SDVO are operating simultaneously

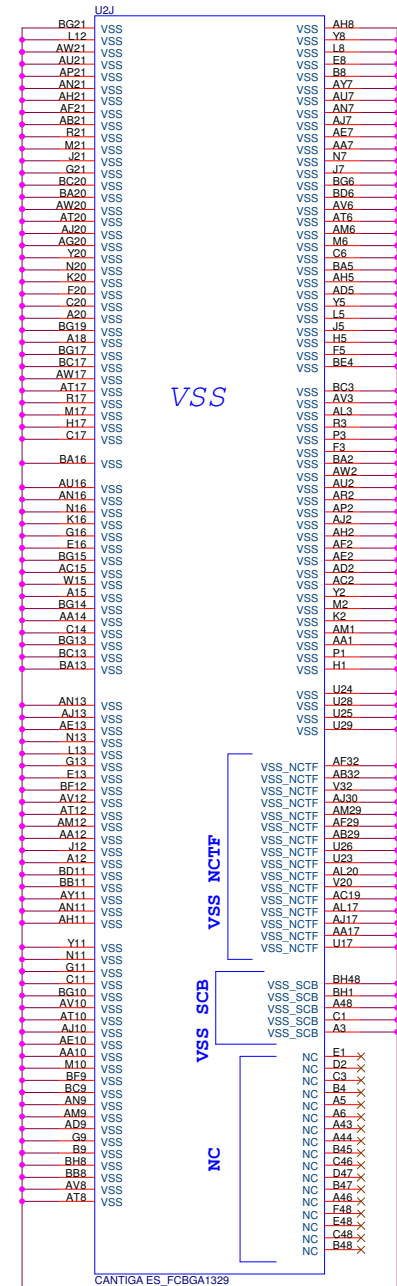
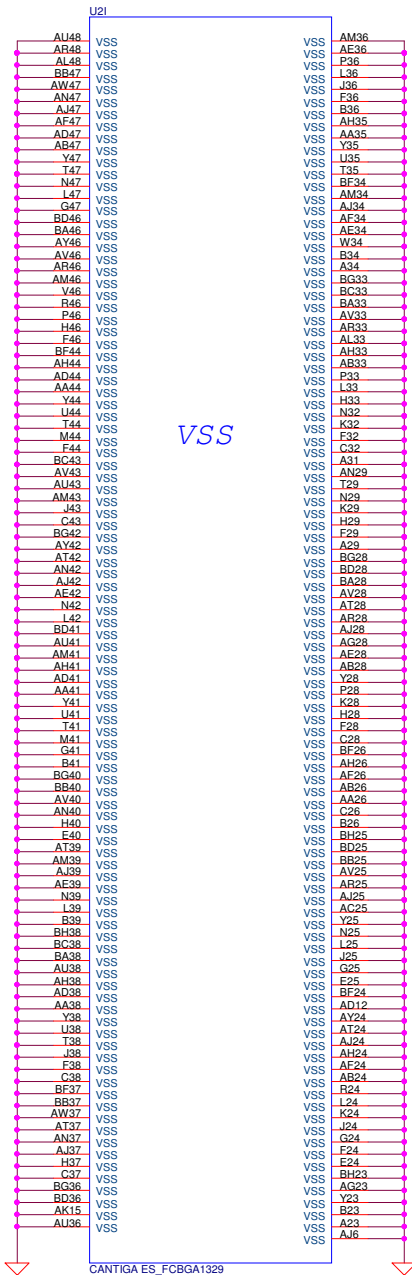


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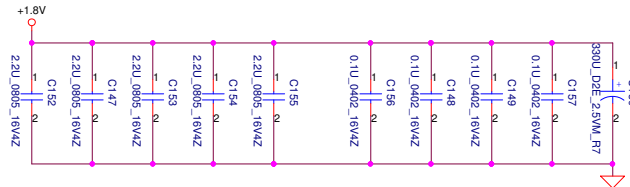


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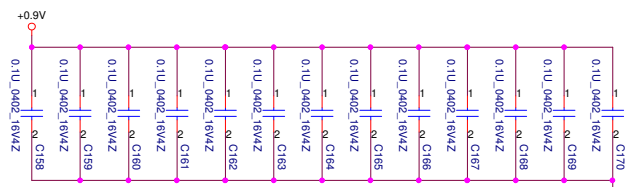




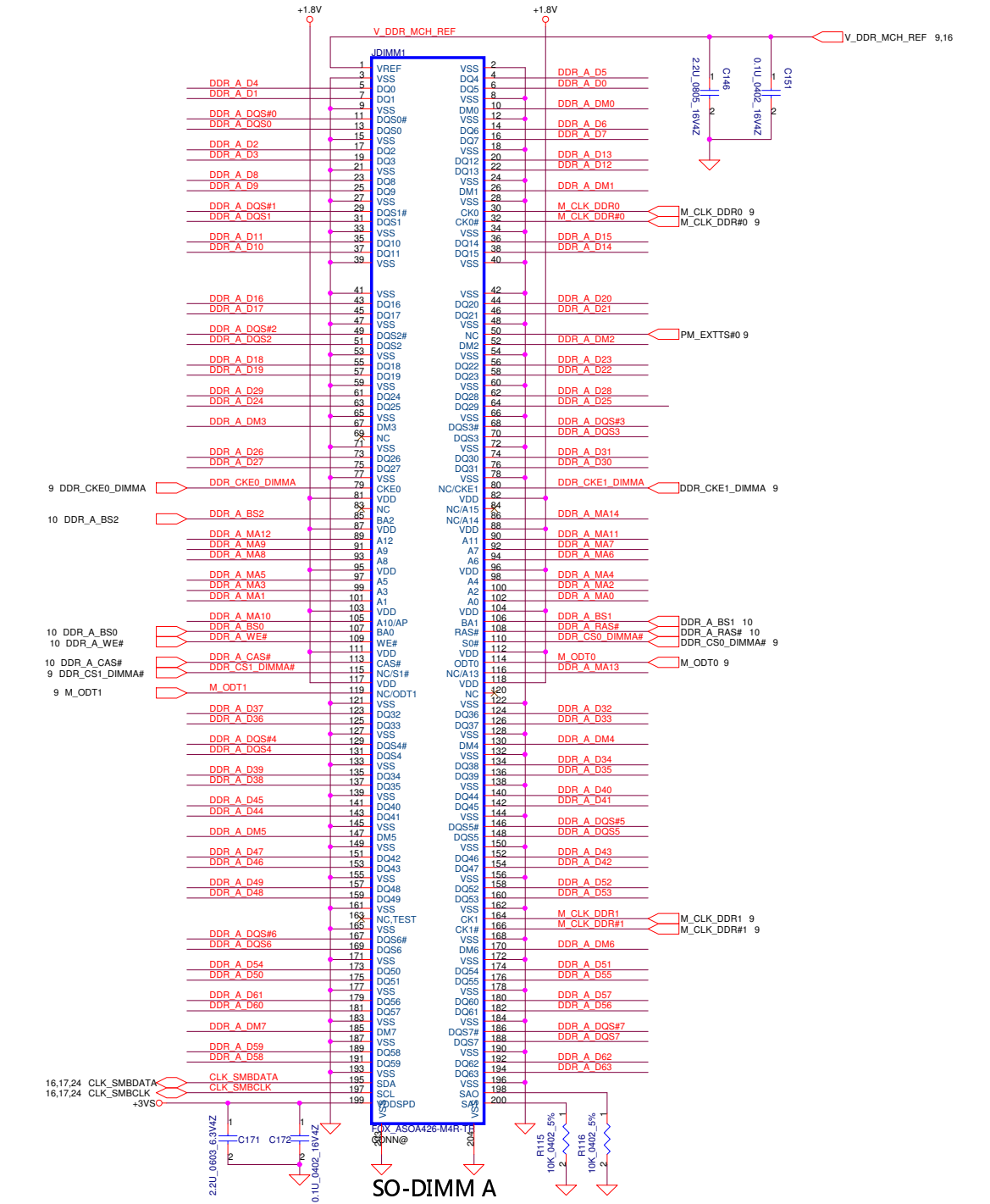
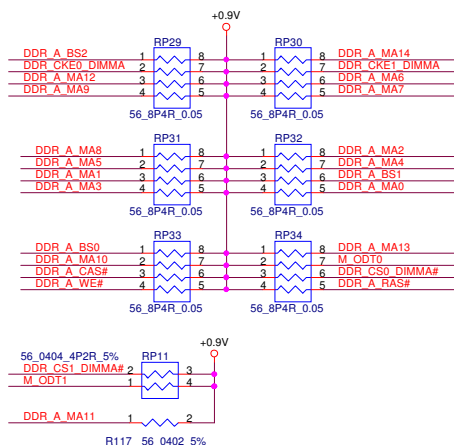
Layout Note:  
Place near  
JP3



Layout Note:  
Place one cap close to every 2  
pullup  
resistors terminated to +0.9V5

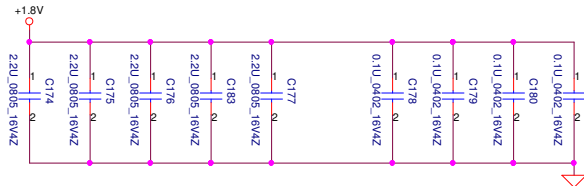


Layout Note:  
Place these resistor  
closely JP3, all  
trace length Max=1.5"

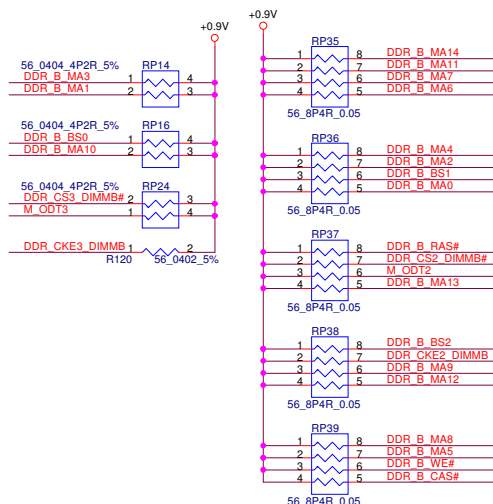
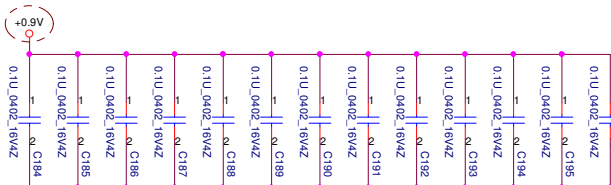


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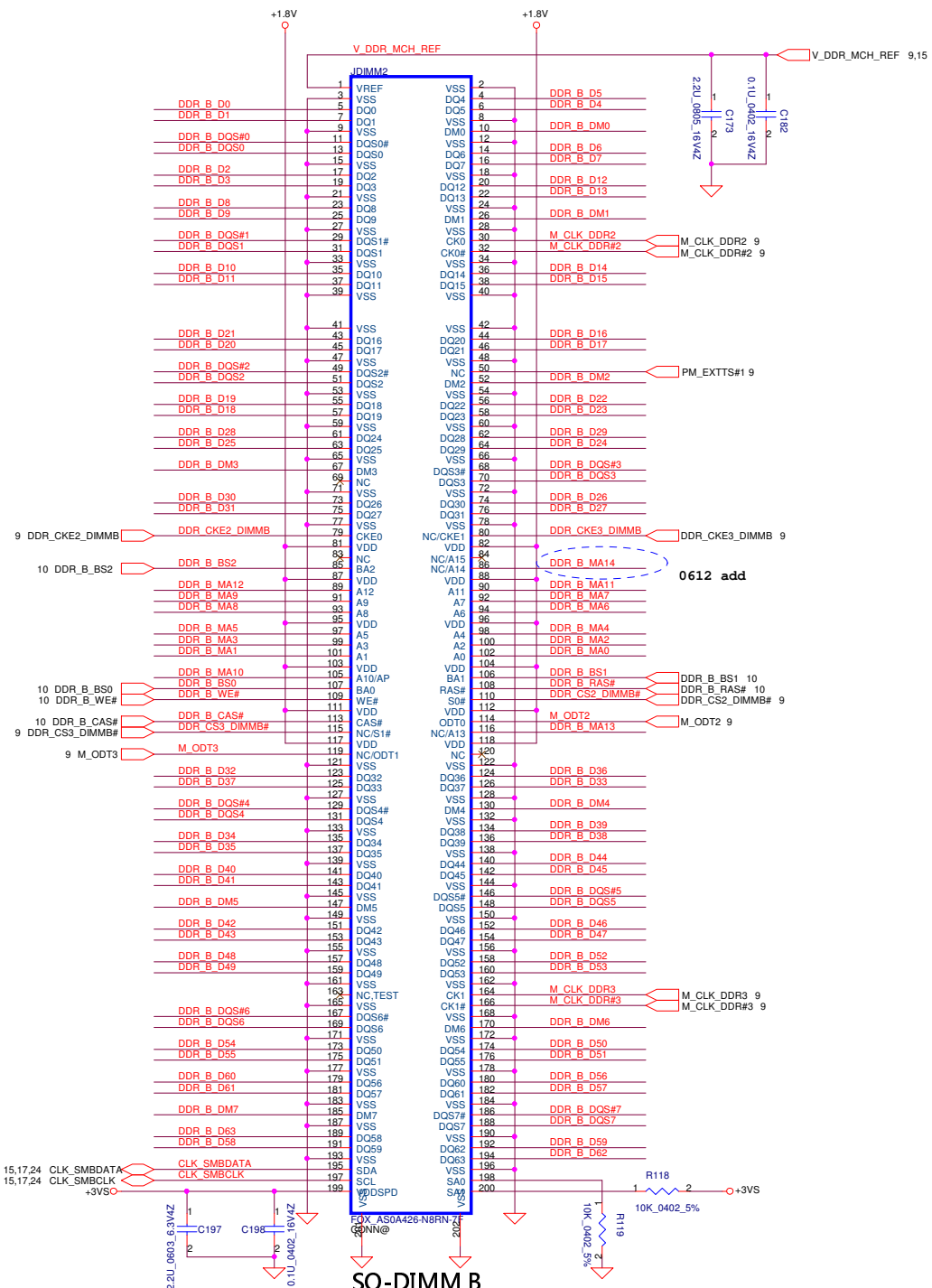
Layout Note:  
Place near  
JP10



Layout Note:  
Place one cap close to every 2  
pullup  
~~resistors terminated to +0.9VS~~



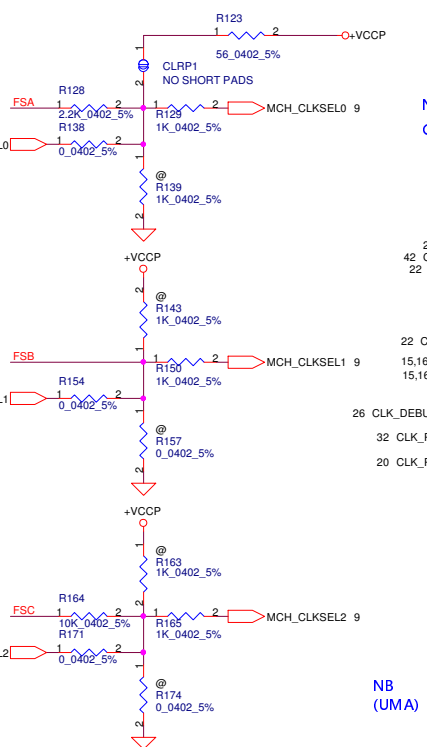
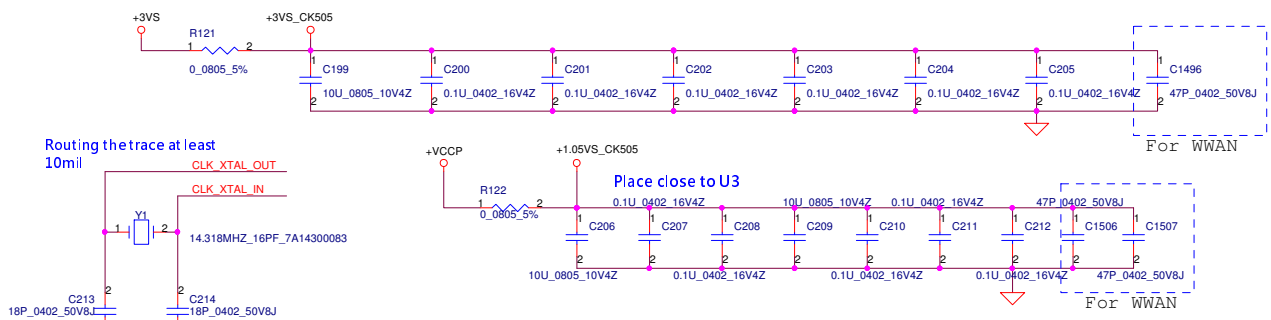
**Layout Note:**  
Place these resistor  
closely JP3,all



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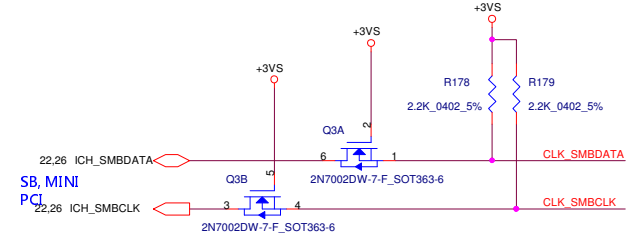
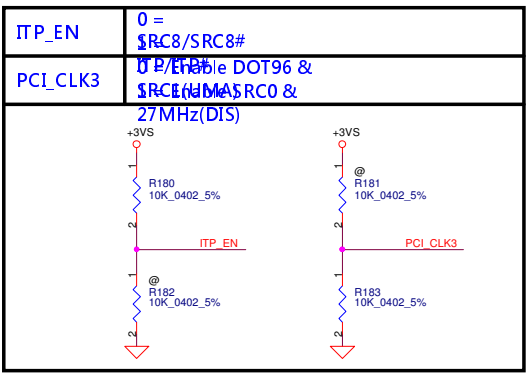
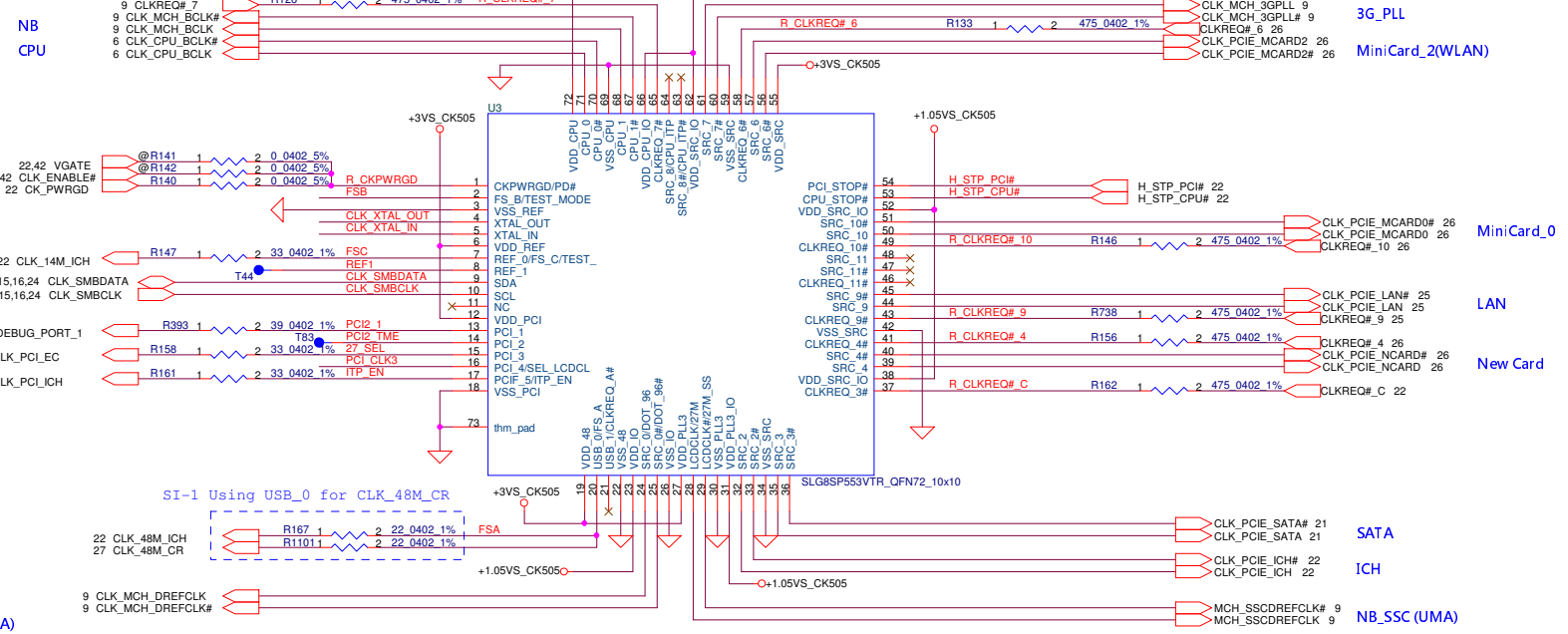


FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



NB  
CPU

NB  
(UMA)

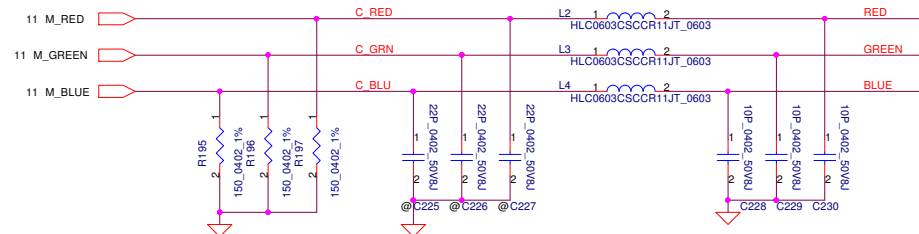


EMI			
@C1482	2	1	CLK 48M_CR
5P_0402_50V8C	2	1	CLK 48M_ICH
5P_0402_50V8C	2	1	CLK 14M_ICH
C216	2	1	CLK PCI_ICH
12P_0402_50V8J	2	1	CLK PCI_EC
@C217	2	1	CLK PCI_EC
47P_0402_50V8J	2	1	CLK DEBUG_PORT_1
@C218	2	1	CLK PCI_EC
47P_0402_50V8J	2	1	CLK PCI_EC
@C219	2	1	CLK PCI_EC
47P_0402_50V8J	2	1	CLK PCI_EC

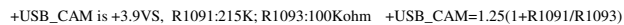
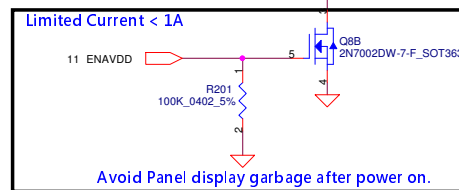
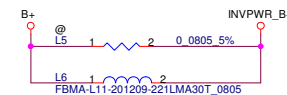
Install C217,C218,C219 for WWAN noise

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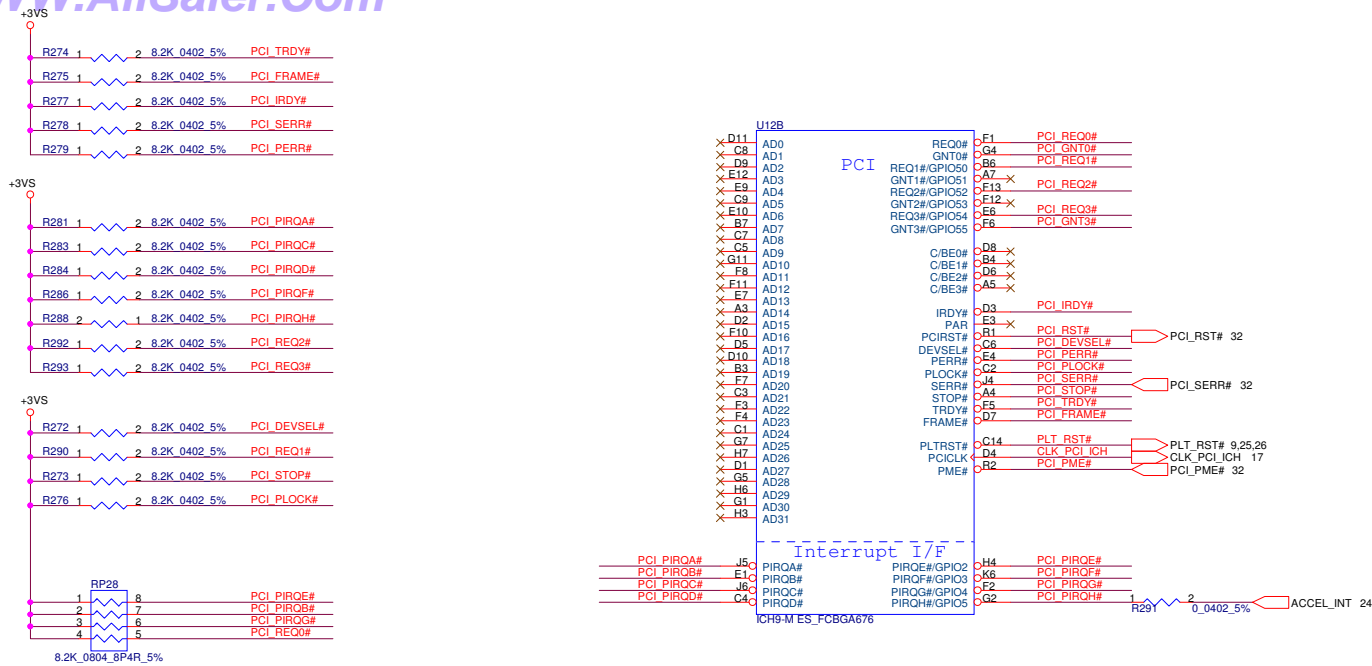
WWW.AliSaler.Com



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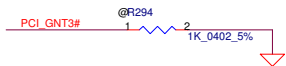


FINAL OF R&D NS	Document Number <b>Montevina UMA</b>	Rev 0.1
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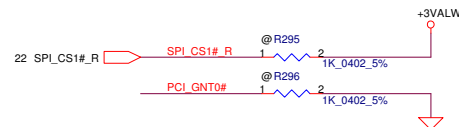
### A16 swap override Strap

PCI_GNT3#	Low= A16 swap override Enble High= Default*
-----------	--



### Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

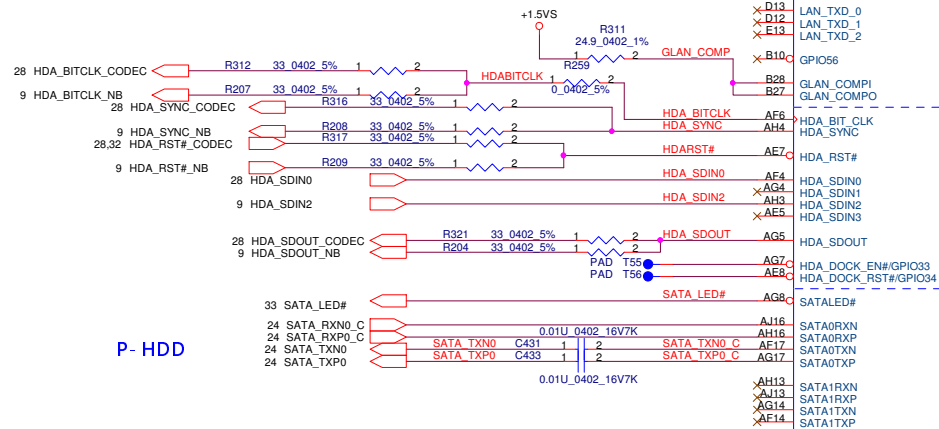
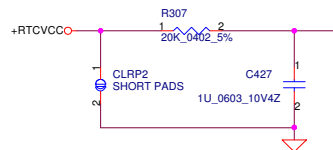
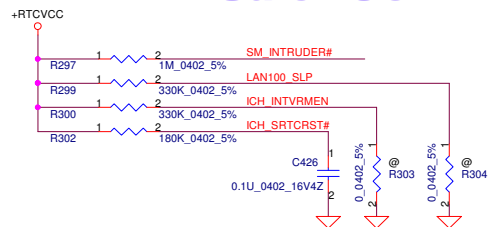


ICH9M Internal VR Enable Strap  
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH\_INTVRMEN Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

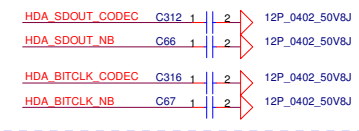
ICH9M LAN100 SLP Strap  
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH\_LAN100\_SLP Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

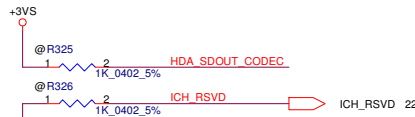


P-HDD

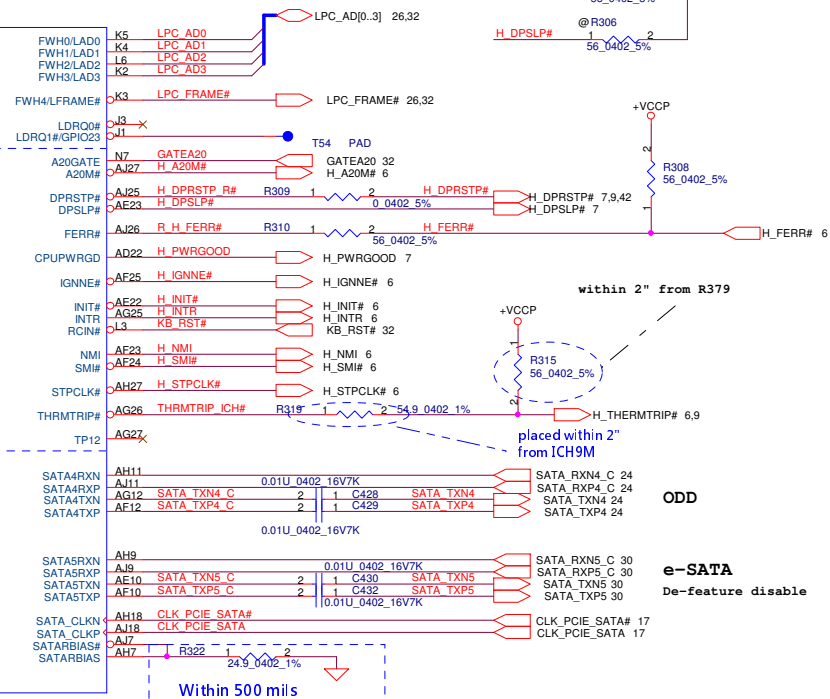
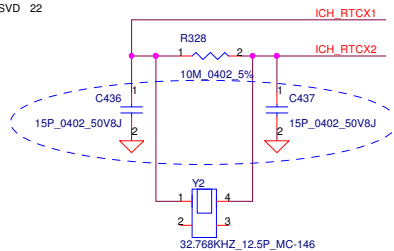
Add 12p on HDA\_SDOOUT and HDA\_SDOOUT  
Add 12p on HDA\_BITCLK\_CODE and HDA\_BITCLK\_NB



XOR CHAIN ENTRANCE STRAP:RSVD



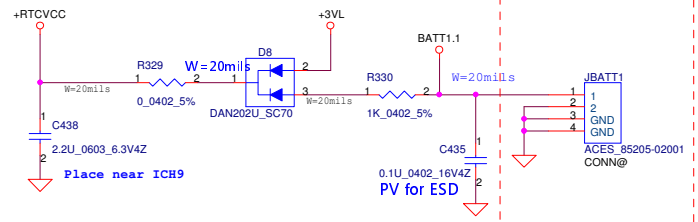
ICH_RSVD	HDA_SDOOUT_CODE
0	0
0	1
1	0
1	1



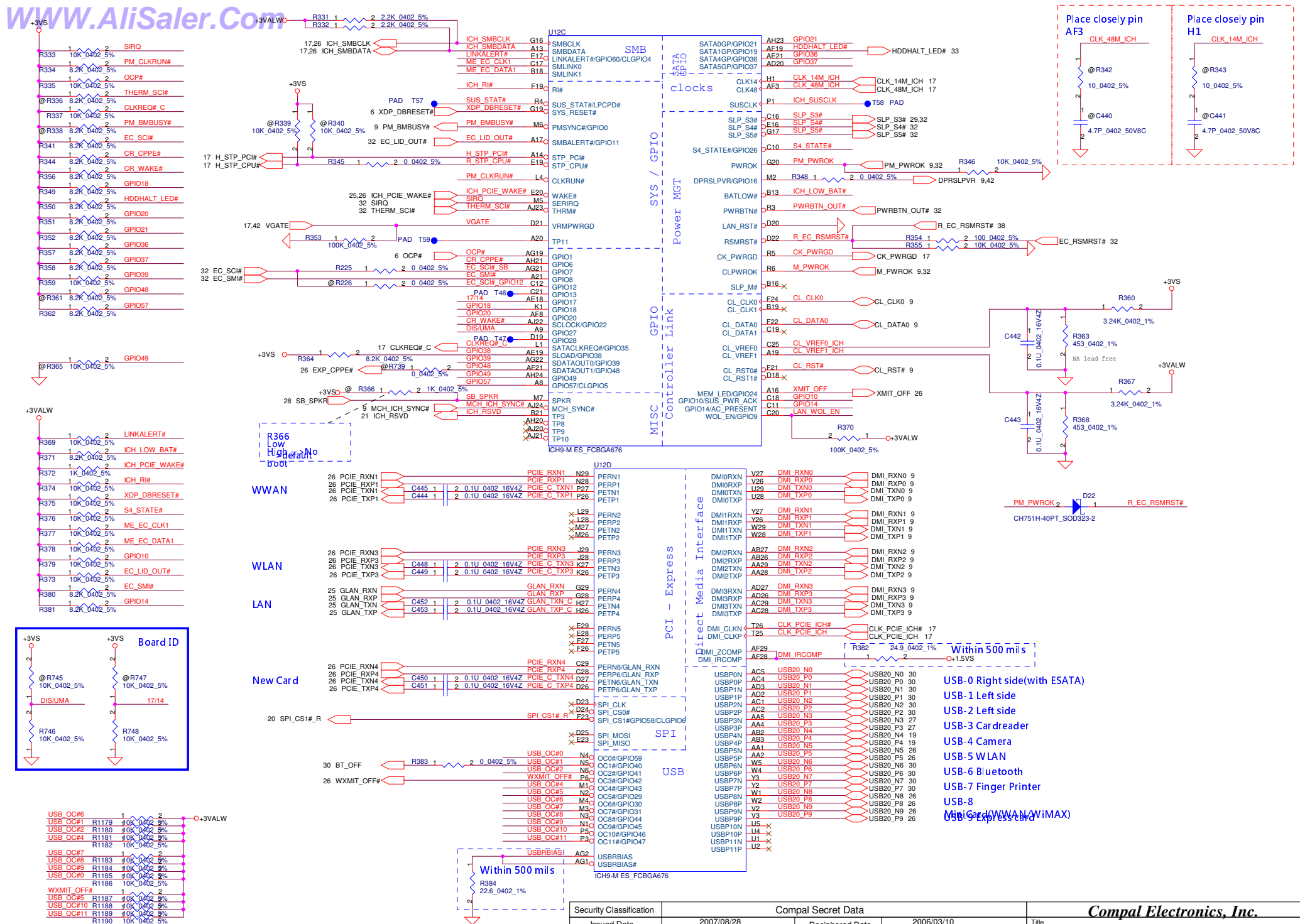
e-SATA  
De-feature disable

Within 500 mils

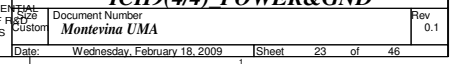
Reserve cap on HDA\_BITCLK for WWAN noise issue



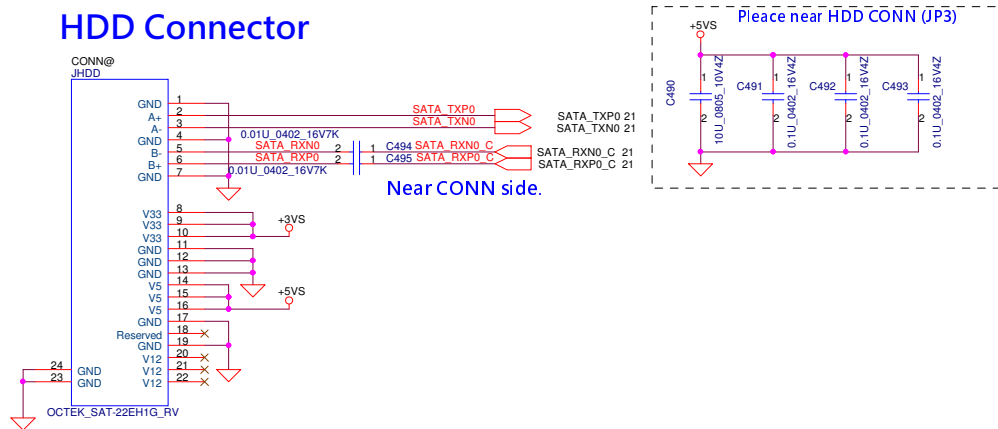
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Compal Electronics, Inc.		
ICH9(2/4) LAN,HD,IDE,LPC		
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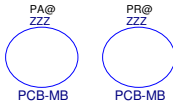
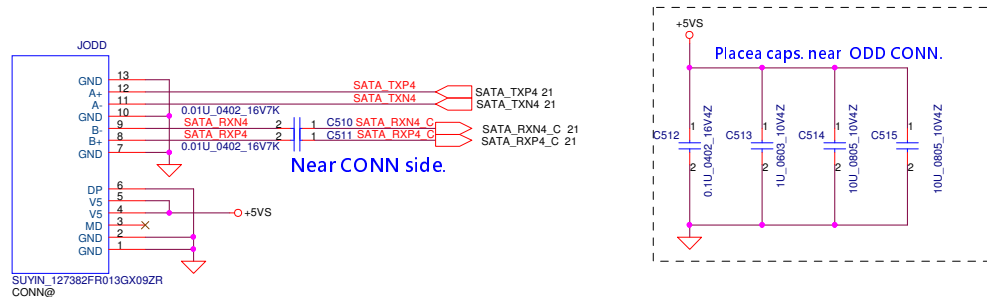




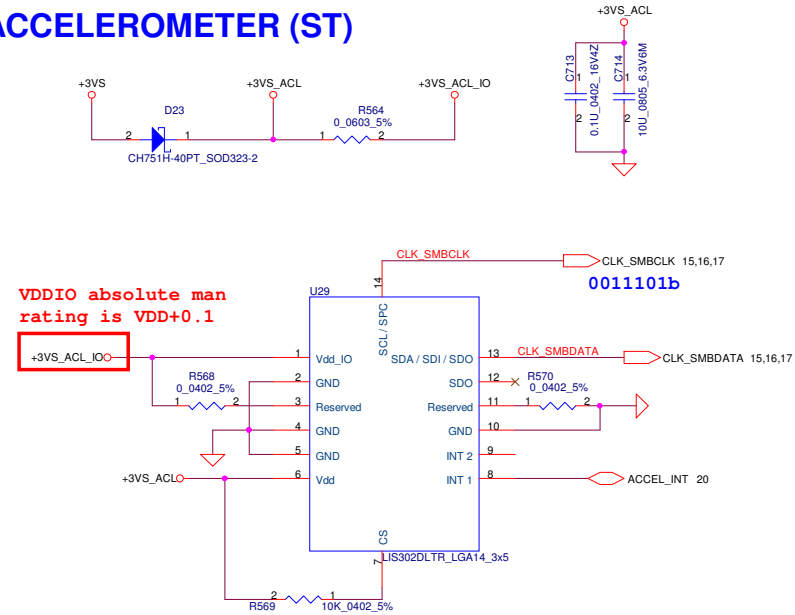
## HDD Connector



## CD-ROM Connector

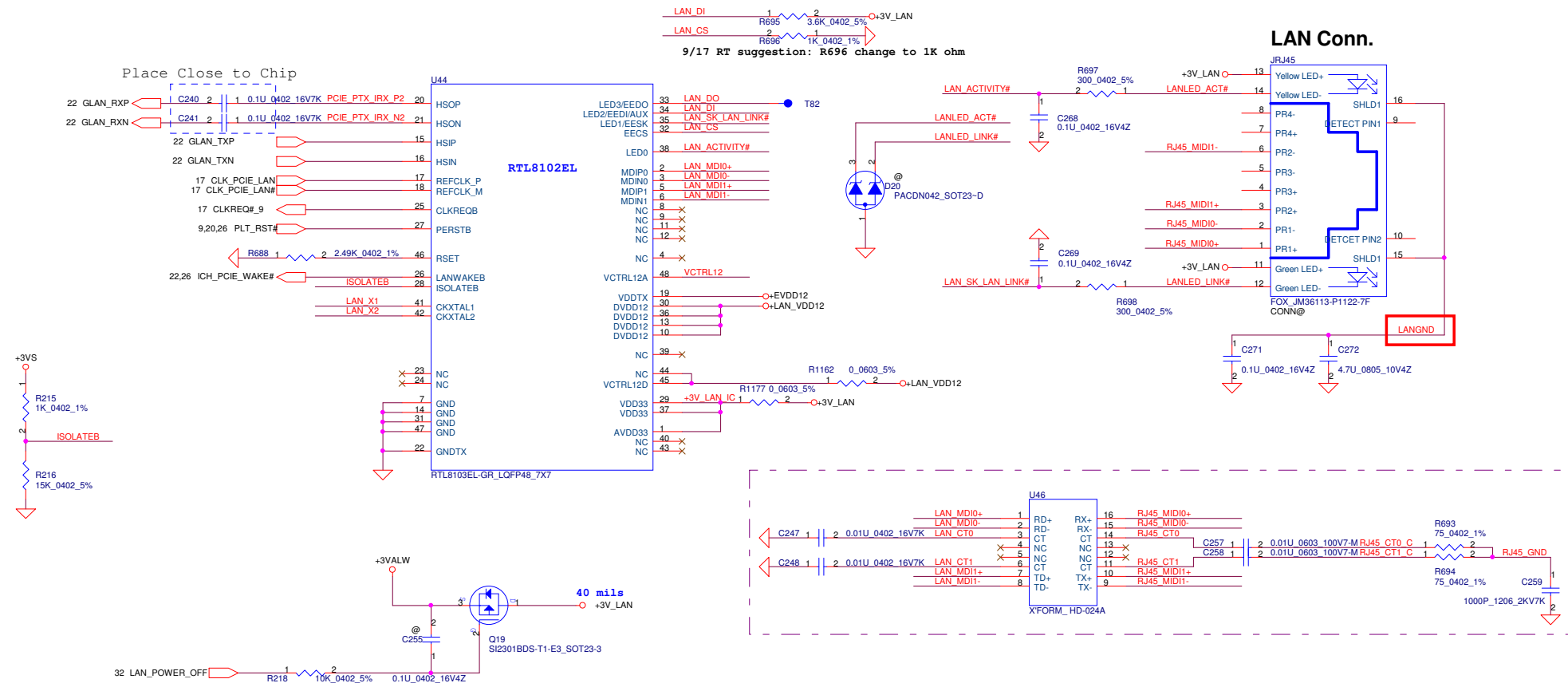


## ACCELEROMETER (ST)

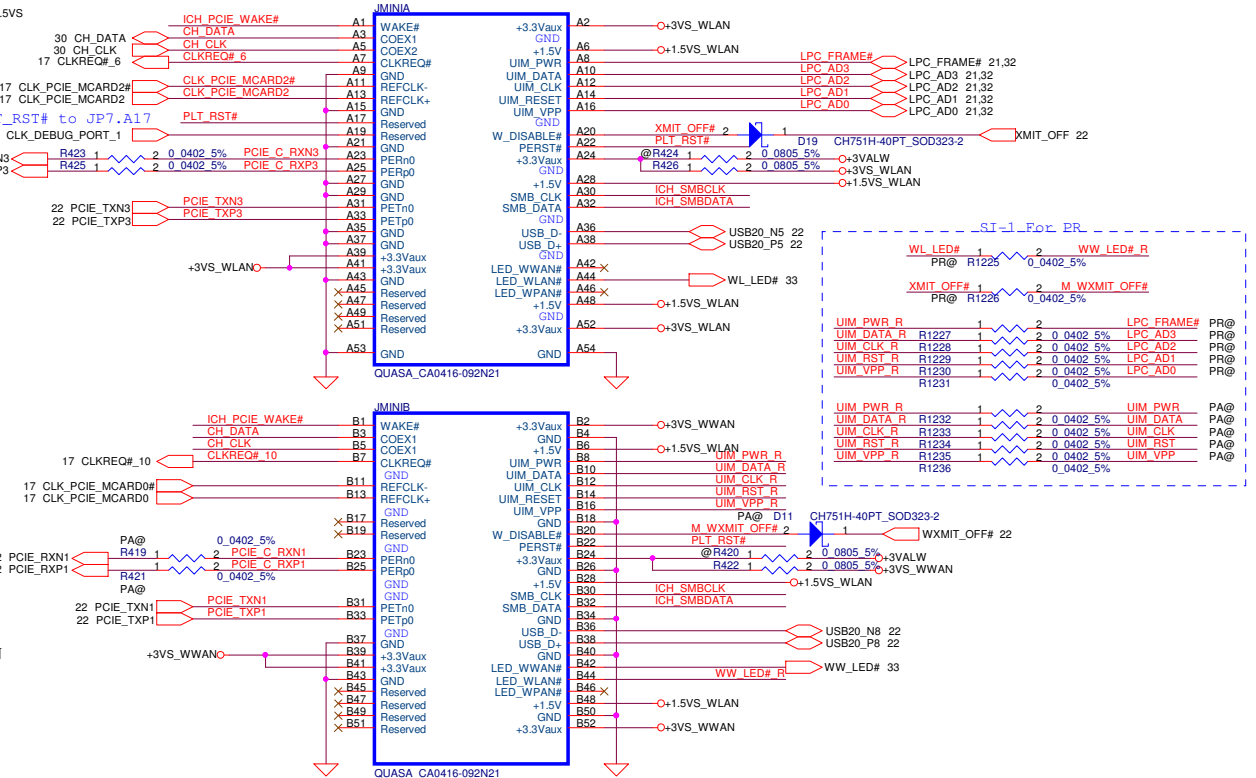


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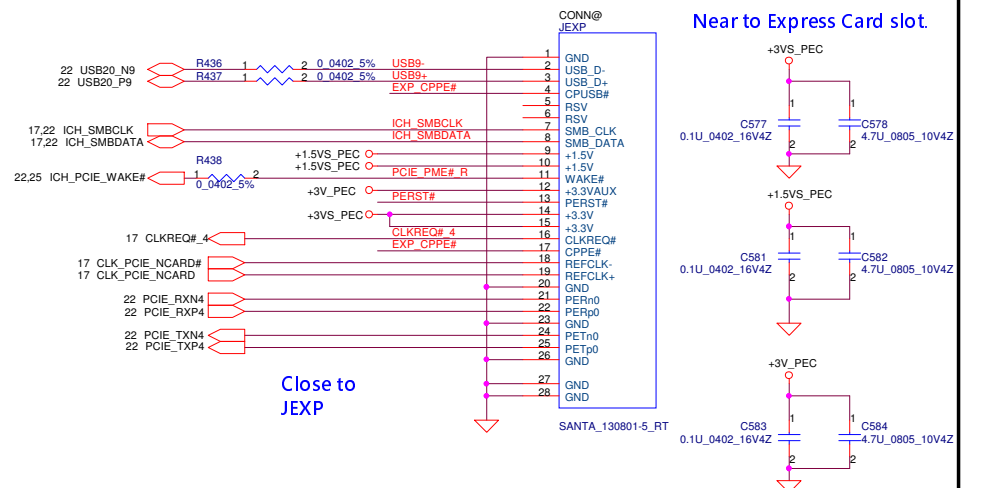


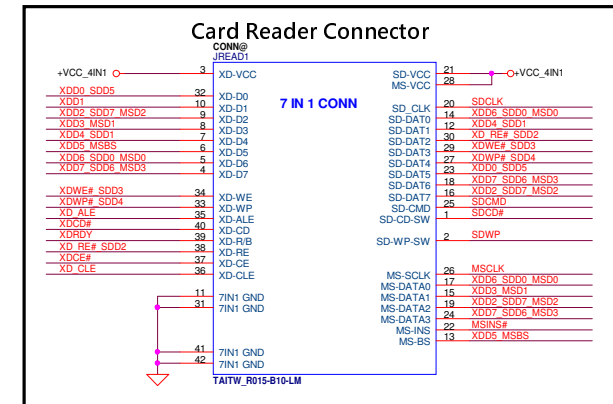
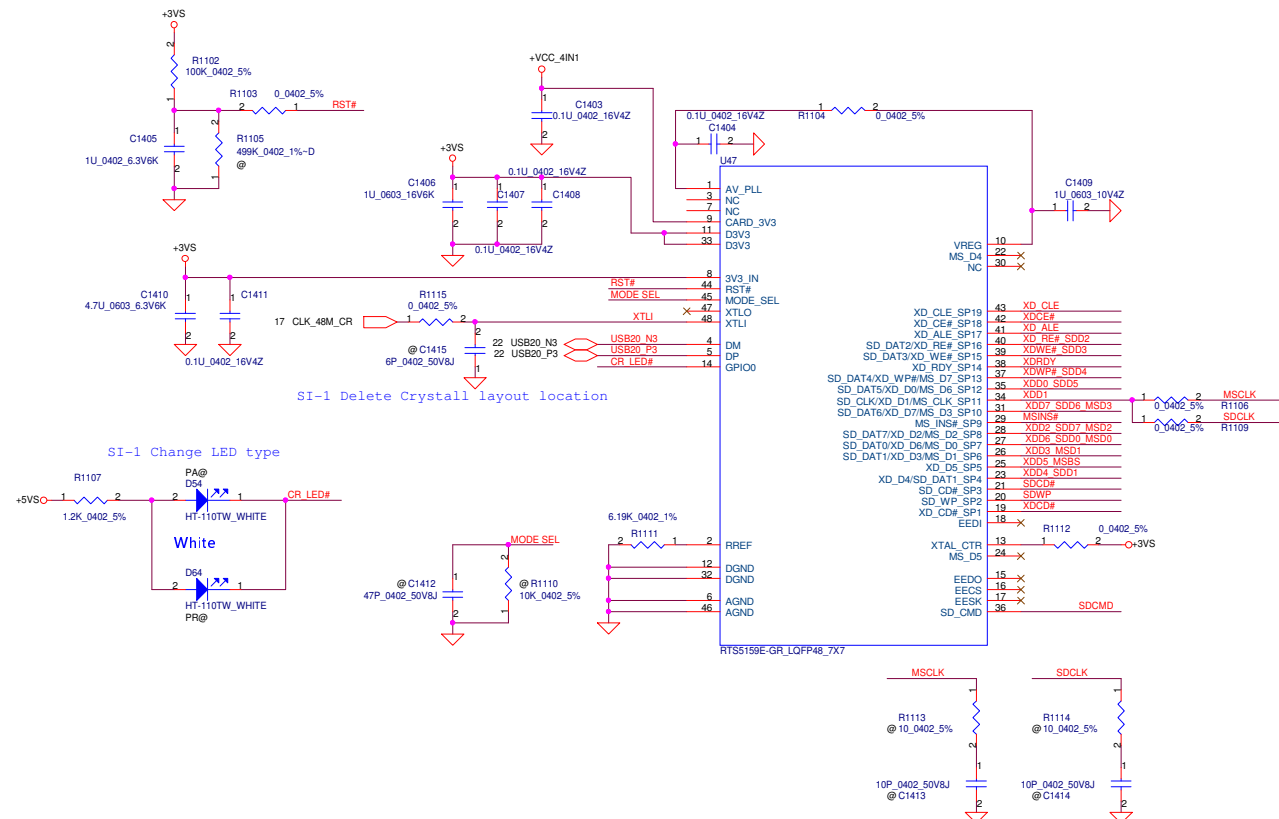


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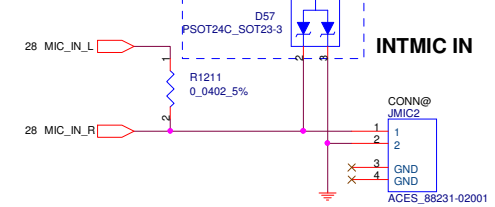
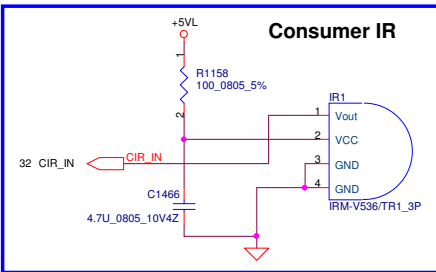
internal pull high to 3.3Vaux-in  
EC need setting at Hi-Z & output Low





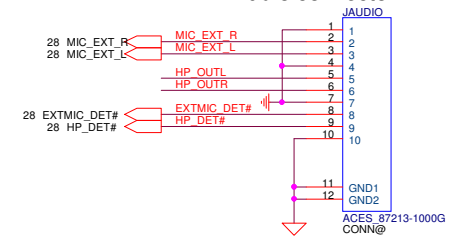


GAIN1	GAIN0	Av (inv)
0	0	10dB
0	1	12dB
1	0	<b>v</b> 15.6dB
1	1	21.6dB



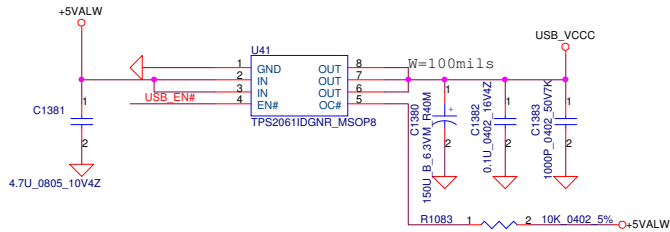
SI-1 Add Audio board connector

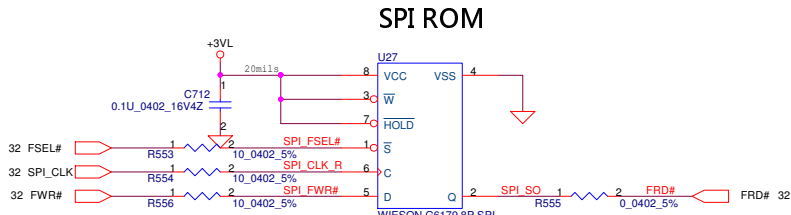
### Audio connector



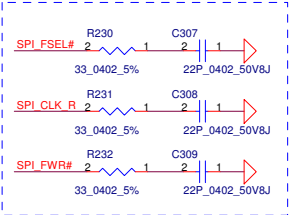
Security Classification	Compal Secret Data					
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Title	AMP & Audio Jack	
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## Right side USB Power Switch

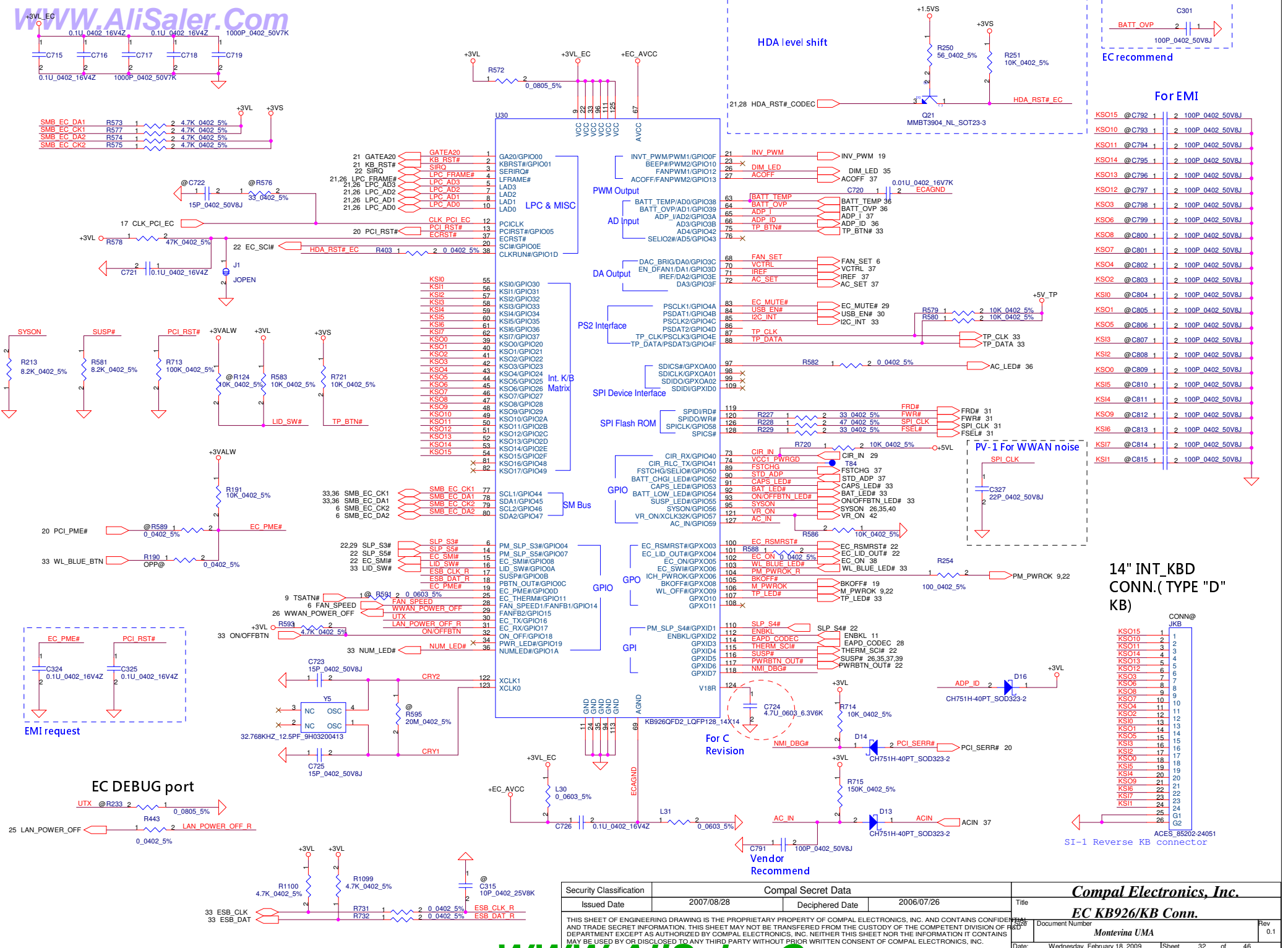




SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH  
WIESO\_G6179-100000\_8P



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Issued Date	2007/08/28	Deciphered Date	2006/07/26	BIOS ROM	
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				Montevina UMA	0.1
				Date: Wednesday, February 18, 2009	Sheet 31 of 46

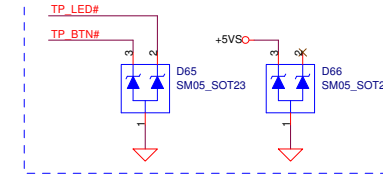




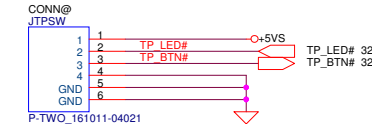
SI-1 Delete SW2

Power Button  
for debug only

MV-1 For ESD request, close to JTPSW

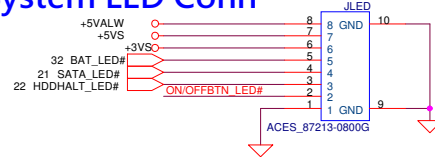


T/P Board (Include T/P\_ON/OFF)

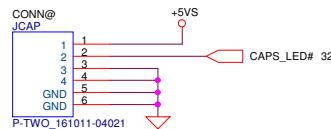


System LED Conn

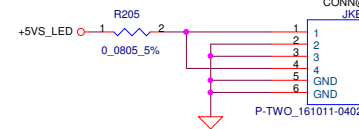
White  
AMBER



Caps-Lock Conn

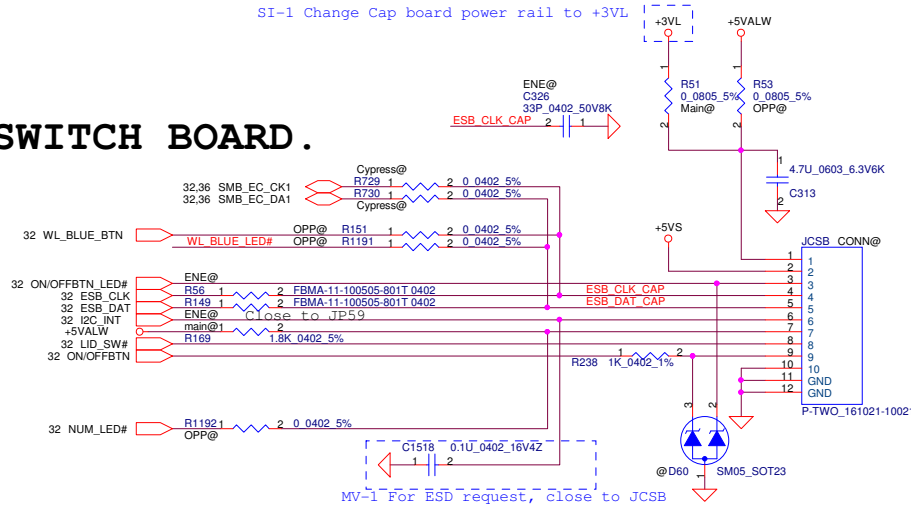


Keyboard backlight Conn

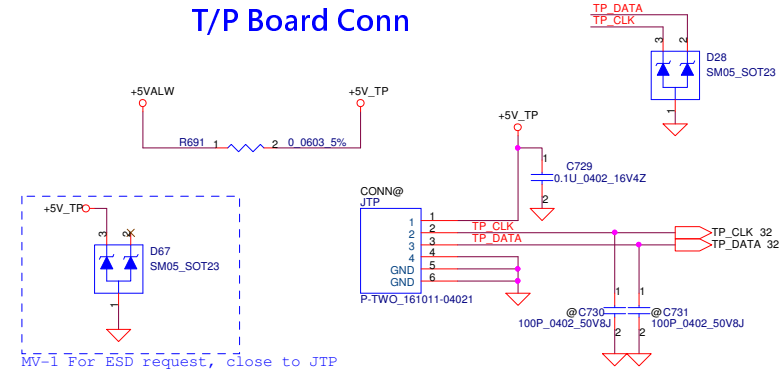


SWITCH BOARD.

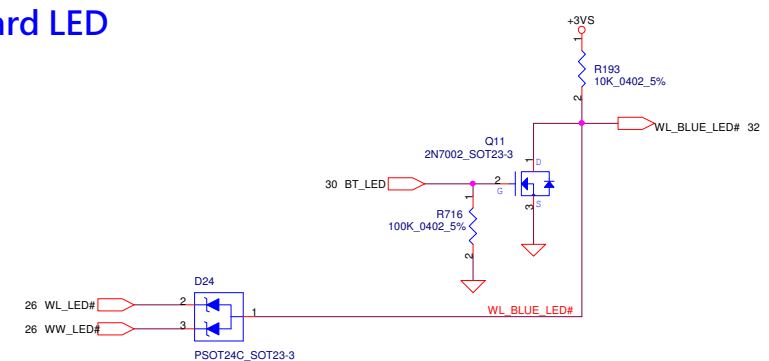
SI-1 Change Cap board power rail to +3VL



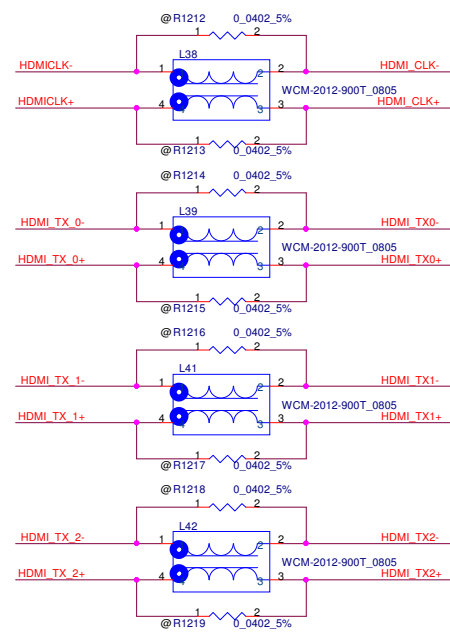
T/P Board Conn



Mini card LED

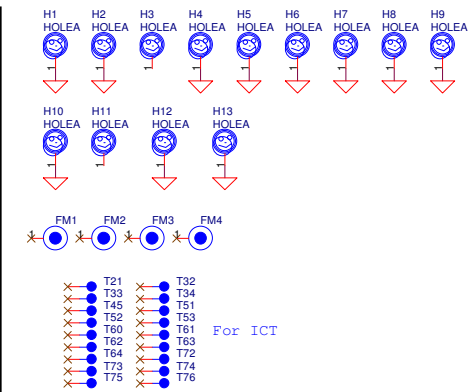
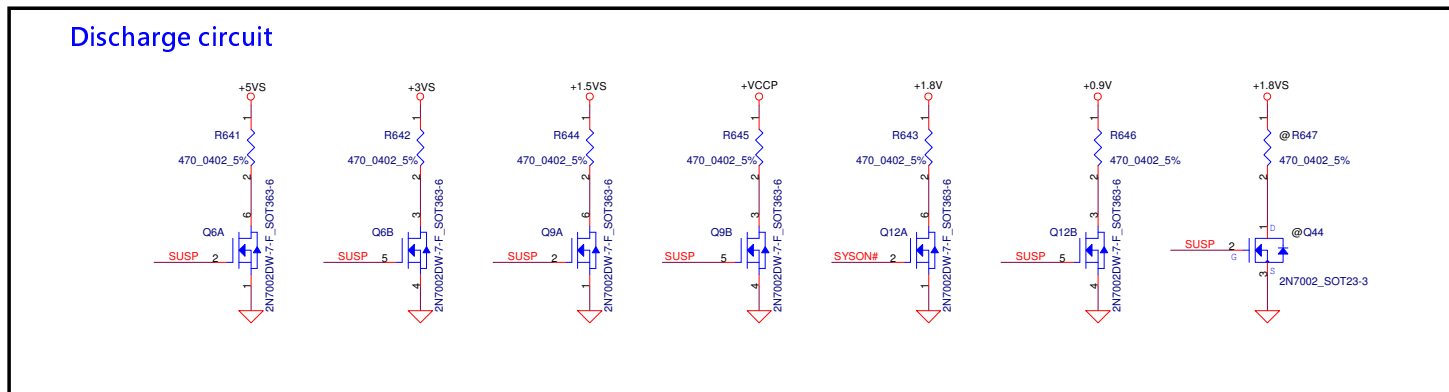
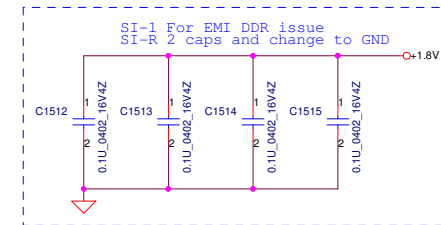
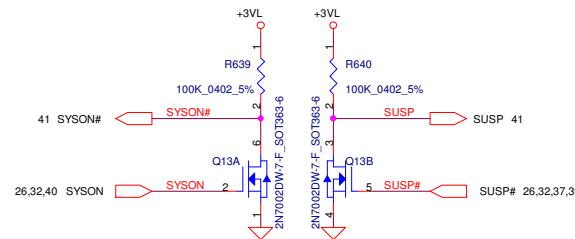
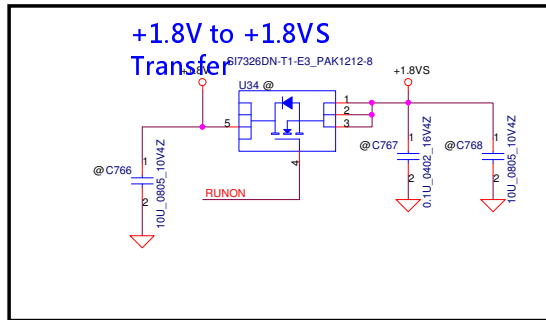
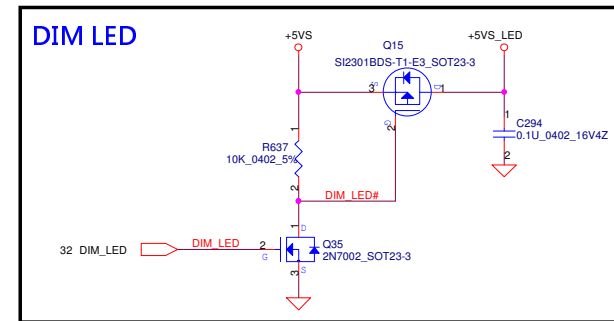
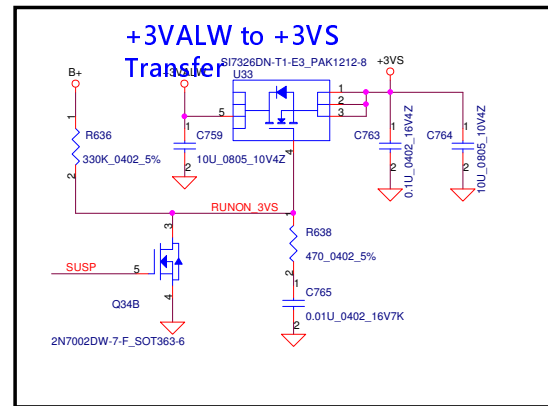
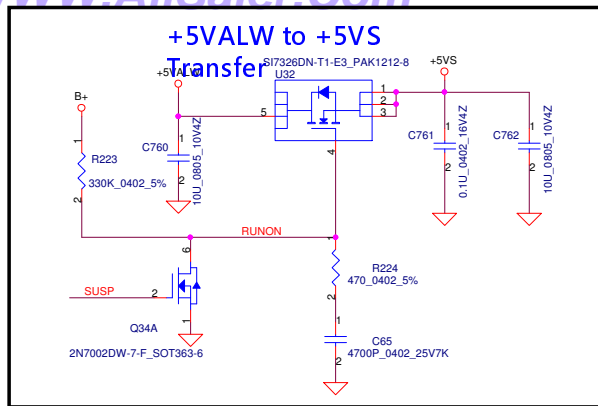


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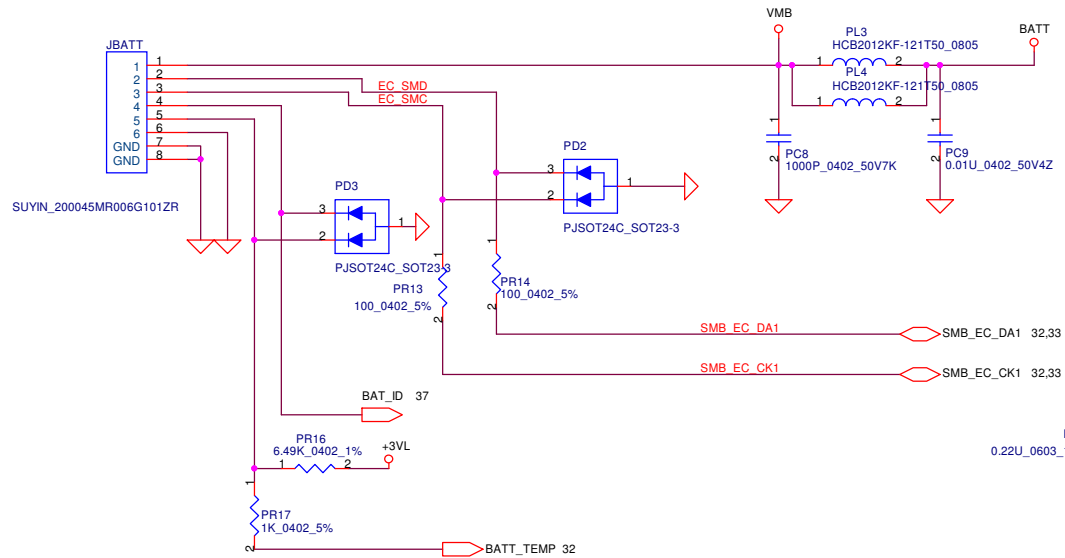
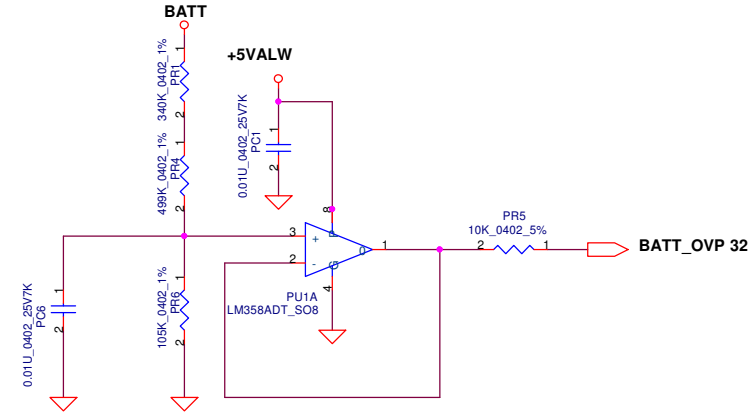
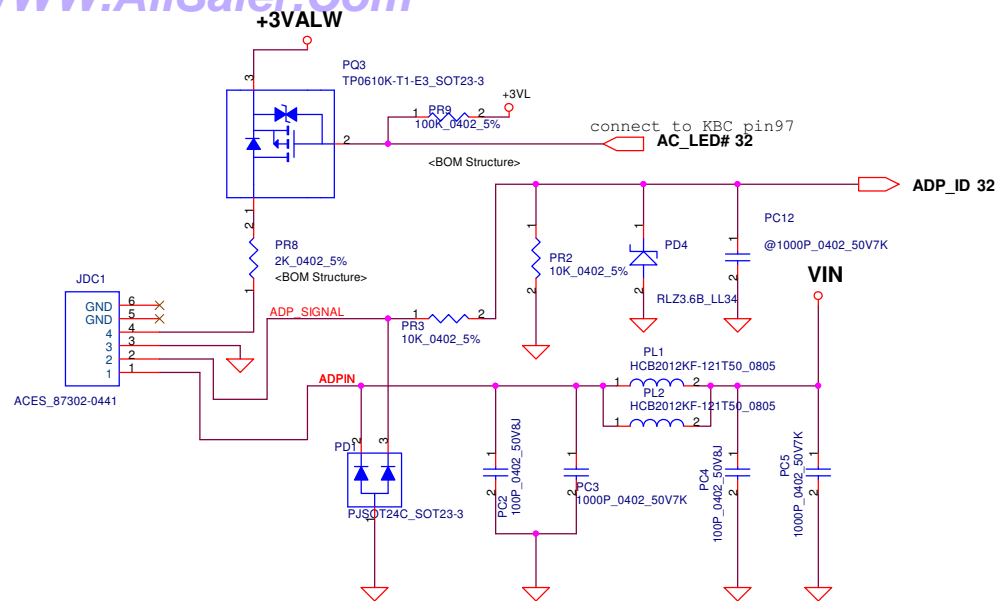


	ST	Parade 81011	Parade 8171
R1240	X	X	X
R1242	0 ohm	0 ohm	4.7K ohm
R1201	X	4.7K ohm	X
R1204	4.7K ohm	X	4.7K ohm
R1243	X	X	4.7K ohm
R1244	X	X	X
R653	3.9K ohm	499 ohm	499 ohm
R1206	0 ohm	X	X
C1517	X	X	2.2uF
R1248	0 ohm	0 ohm	X
R1250	X	X	4.7K ohm
R1251	X	X	4.7K ohm
R1252	0 ohm	0 ohm	X
R1247	X	X	4.7K ohm
R1249	0 ohm	0 ohm	X
R1245	0 ohm	0 ohm	X
R1246	X	X	4.7K ohm
R1203	0 ohm	X	4.7K ohm
R1241	X	X	X
R1205	0 ohm	X	X
R1202	X	X	4.7K ohm
C773	0.1uF	1uF	1uF
R1207	V	X	X
R1208	V	X	X

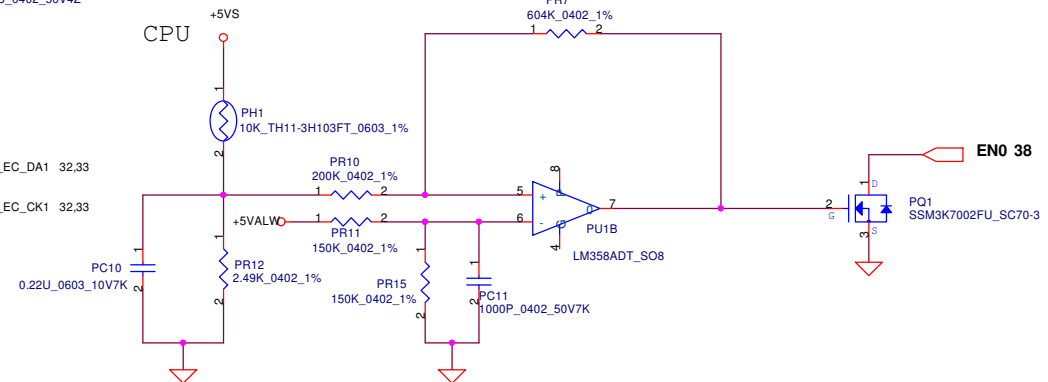
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>HDMI LS &amp; Conn.</b>	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	
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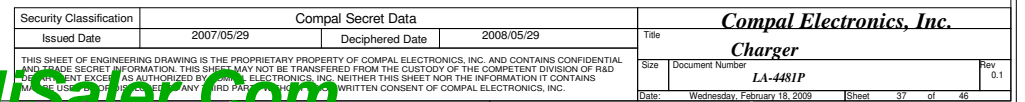
Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	DC/DC Interface	
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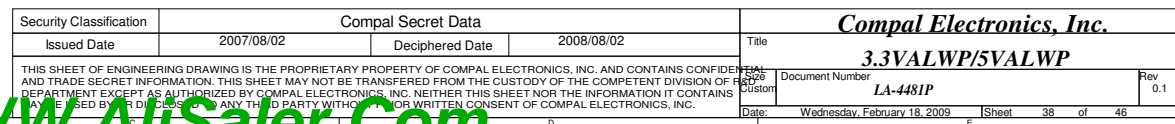


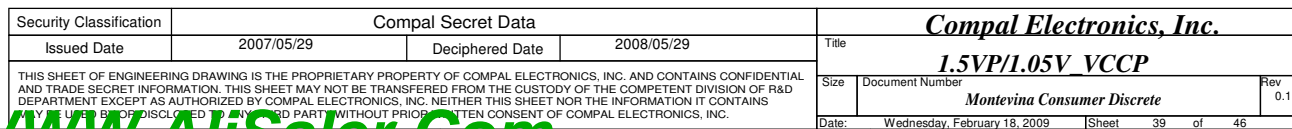
PH1 under CPU botten side :  
CPU thermal protection at 90  $\pm$  3 degree C

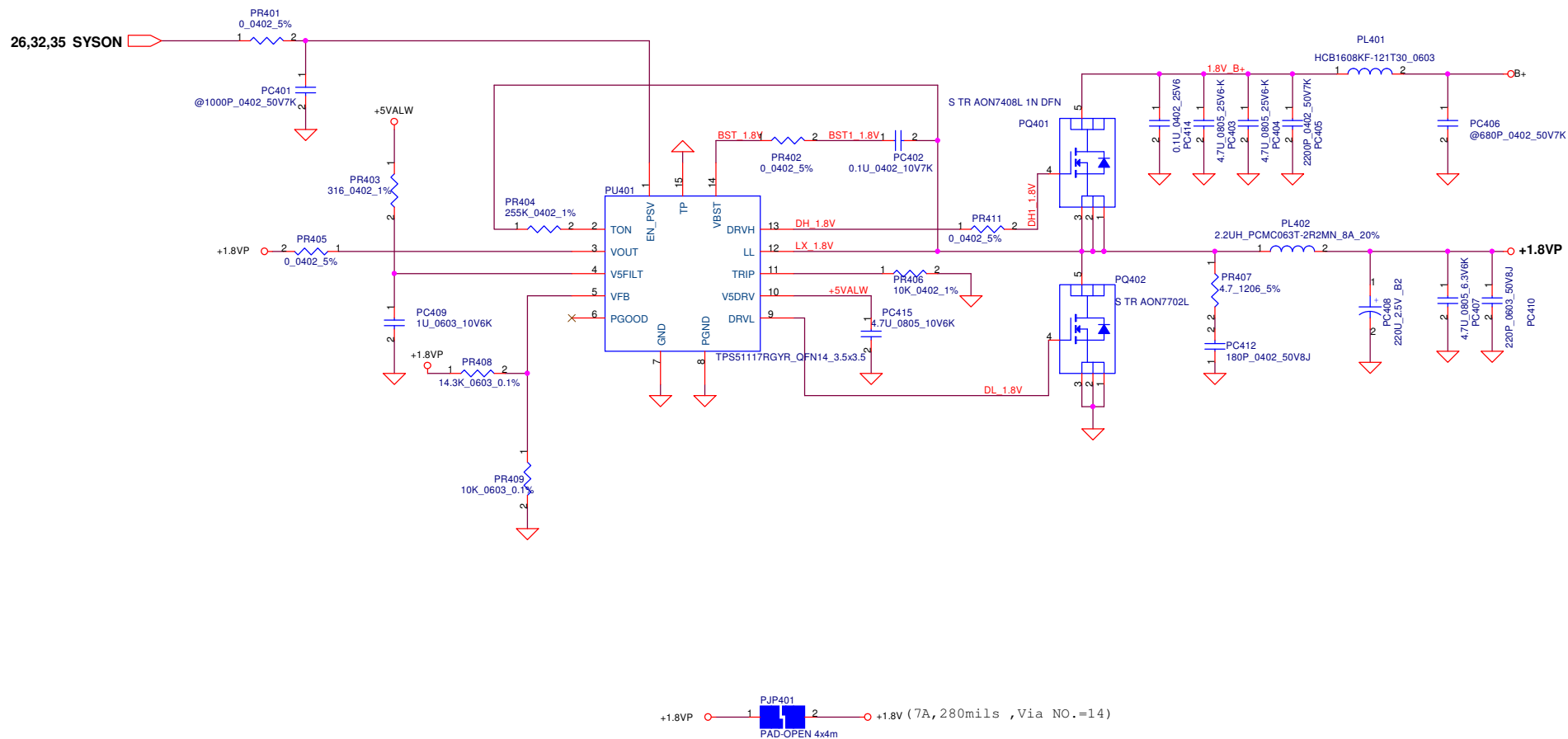


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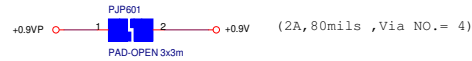
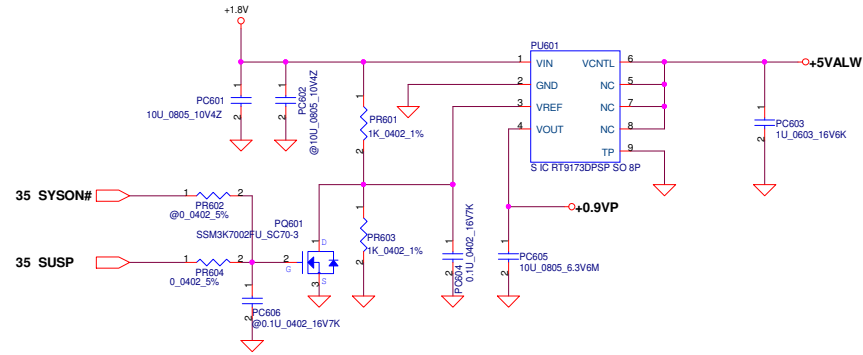




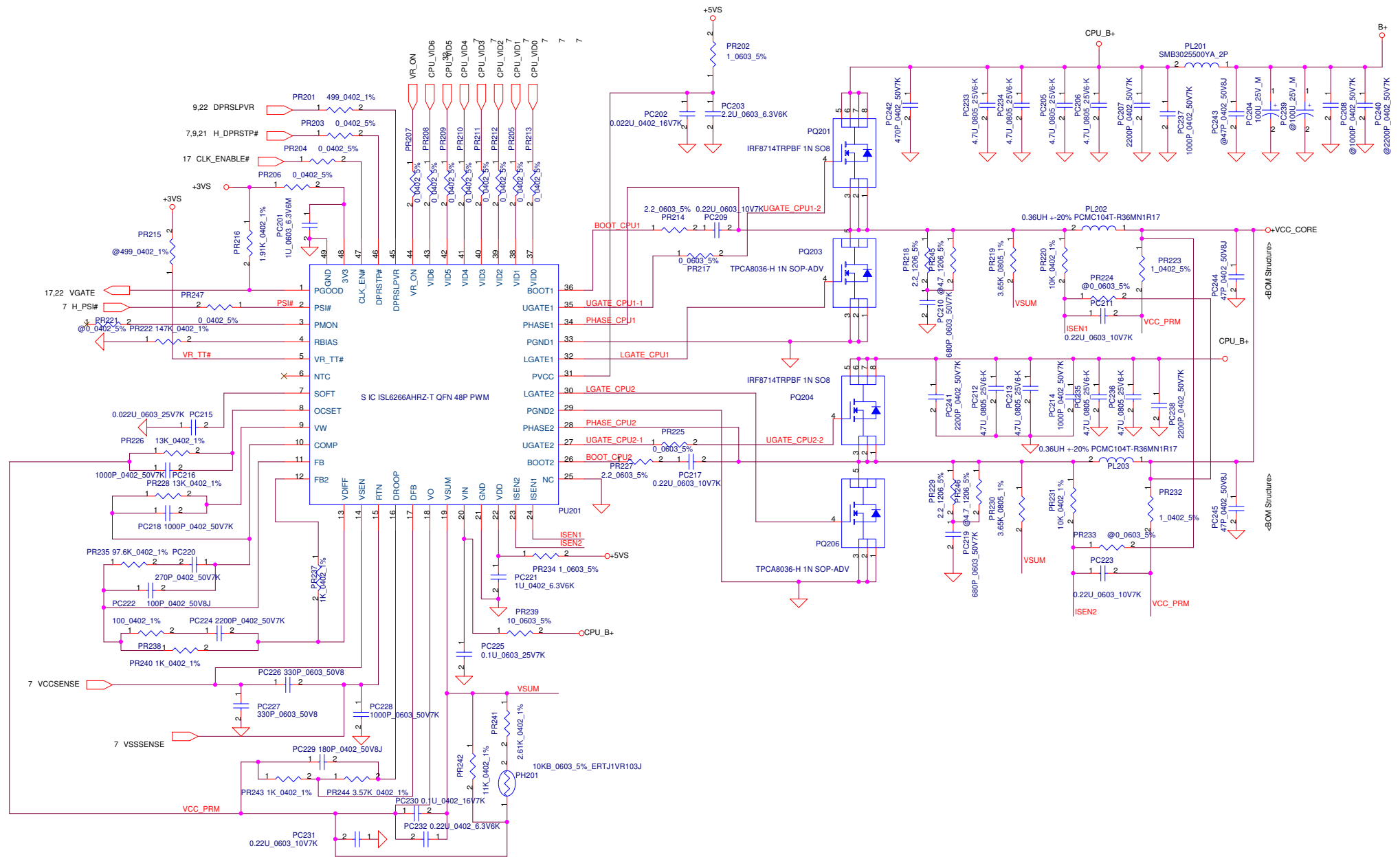


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Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title	
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Compal Electronics, Inc.

+CPU\_CORE

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							

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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title			
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	CardReader clock issue	17	Using USB_0 for CLK_48M_CR	2008/10/08	SI-1
2	Debug Card issue	26	Connect PLT_RST# to JP7.A17	2008/10/08	SI-1
3	SMT issue	29	Change IR1 to SCR00000E00	2008/10/08	SI-1
4	Add Audio board	29	Add JAUDIO for audio board	2008/10/08	SI-1
5	SW2 is for DB1 debug	33	Delete SW2	2008/10/08	SI-1
6	Cap board issue	33	Change Cap board power rail to +3VL	2008/10/08	SI-1
7	Support GM47	13	Add C1503 for GM47	2008/10/08	SI-1
8	Change FAN control circuit to voltage control	6	Add U51,D63	2008/10/08	SI-1
9	Delete HDA SSC	21	Remove U8 for layout spacing	2008/10/08	SI-1
10	For PR mini card connector	26	Add R1225 -- R1236	2008/10/08	SI-1
11	PA/PR CardReader LED	27	D54 for PA, D64 for PR	2008/10/08	SI-1
12	EMI request	28	Change R1132 to bead	2008/10/08	SI-1
13	Use audio board	29	Add audio board connector, change WIC to 2pin and add SPK connector	2008/10/08	SI-1
14	Change JFPR to 6 pin connector	30	Add Q109, C1518, R1210	2008/10/08	SI-1
15	EMI request	35	Add C1512 -- C1517	2008/10/08	SI-1
16	Change JFPR to 4 pin connector	30	Delete Q109, C1518, R1210	2008/11/21	SI-R
17	Delete resistor for Debug card	26	Delete R1220-R1224	2008/11/21	SI-R
18	EMI request	35	Delete C1516,C1517 and connect to GND	2008/11/21	SI-R
19	For Intel DPST	19	Add R1237,R1238	2008/11/25	SI-R
20	EMI and WWAN request	17 28	Install C217, C218, C219, C435, C312, C316, C66, C67, C1478, C1479, C1480, C1481, D58, C1516, R1239, C327	2008/12/18	PV-1
21	Audio board connector	29	Change pin define	2008/12/18	PV-1
22	ST and Parade level shift	34	Add R for Parade	2008/12/18	PV-1
23	ESD request	33	Add C1518,D65,D66,D67	2008/1/19	MV-1
24	ESD/ EMI request	17 38	C217-C219, D5-D7, D45-D47, D20, C792-C815 no stuff	2008/2/13	MV-1
25	AUDIO issue	29	C1446, C1447 change to 0805 size	2008/2/13	MV-1
26	PC Beep issue	28	change to analog GND and add separate diode	2008/2/13	MV-1
27					
28					

Item	Fixed Issue	(Reason for change)	PAGE	Modify List	Date	Phase
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Item	Fixed Issue	(Reason for change)	PAGE	Modify List	Date	Phase
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